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A NON-DESTRUCTIVE CROSSBAR ARCHITECTURE OF MULTI-LEVEL
MEMORY-BASED RESISTOR

by

Seyedmorteza Sahebkhorkhorasani

B.S., Sadjad University of Technology, 2011

A Thesis

Submitted in Partial Fulfillment of the Requirements for the
Master of Science

Department of Electrical and Computer Engineering
in the Graduate School
Southern Illinois University Carbondale
May 2015

THESIS APPROVAL

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MEMORY-BASED RESISTOR

By

Seyedmorteza Sahebkhahorasani

A Thesis Submitted in Partial
Fulfillment of the Requirements
for the Degree of
Master of Science
in the field of Electrical and Computer Engineering

Approved by:

Dr. Themistoklis Haniotakis, Chair

Dr. Reza Ahmadi

Dr. Mohammad Sayeh

Graduate School
Southern Illinois University Carbondale
April 4, 2015

AN ABSTRACT OF THE THESIS OF

Seyedmorteza Sahebkhahorasani, for the Master of Science degree in Electrical and Computer Engineering, presented on April 4, 2015, at Southern Illinois University Carbondale.

TITLE:

A NON-DESTRUCTIVE CROSSBAR ARCHITECTURE OF MULTI-LEVEL MEMORY-BASED RESISTOR

MAJOR PROFESSOR: Dr. Themistoklis Haniotakis

Nowadays, researchers are trying to shrink the memory cell in order to increase the capacity of the memory system and reduce the hardware costs. In recent years, there has been a revolution in electronics by using fundamentals of physics to build a new memory for computer application in order to increase the capacity and decrease the power consumption. Increasing the capacity of the memory causes a growth in the chip area. From 1971 to 2012 semiconductor manufacturing process improved from $6\mu\text{m}$ to $22\mu\text{m}$. In May 2008, S. Williams stated that “it is time to stop shrinking”. In his paper, he declared that the process of shrinking memory element has recently become very slow and it is time to use another alternative in order to create memory elements [9].

In this project, we present a new design of a memory array using the new element named Memristor [3]. Memristor is a two-terminal passive electrical element that relates the charge and magnetic flux to each other. The device remained unknown since 1971 when it was discovered by Chua and introduced as the fourth fundamental passive element like capacitor, inductor and resistor [3]. Memristor has a dynamic resistance and it can retain its previous value even after

disconnecting the power supply. Due to this interesting behavior of the Memristor, it can be a good replacement for all of the Non-Volatile Memories (NVMs) in the near future. Combination of this newly introduced element with the nanowire crossbar architecture would be a great structure which is called Crossbar Memristor.

Some frameworks have recently been introduced in literature that utilized Memristor crossbar array, but there are many challenges to implement the Memristor crossbar array due to fabrication and device limitations. In this work, we proposed a simple design of Memristor crossbar array architecture which uses input feedback in order to preserve its data after each read operation.

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TABLE OF CONTENTS

ABSTRACT	i
ACKNOWLEDGMENTS	iii
LIST OF TABLES	v
CHAPTERS	
CHAPTER 1 – Introduction	1
CHAPTER 2 – Background	7
2.1 General Memristor.....	7
2.2 How Memristor works	10
2.3 Pinched Hysteresis.....	12
2.4 Different types of Memristor	14
2.4.1 Titanium Dioxide Memristor	14
2.4.1. a. Titanium Dioxide Memristor	14
2.4.1. b. Polymeric Memristor	15
2.4.1. c. Manganite Memristive System.....	18
2.4.1. d. Resonant Tunneling Diode Memristor	19
2.4.2 Spin Memristive System	19
2.4.3 Three terminal Memristor	22
CHAPTER 3 – Methodology.....	23
3.1 Section-1: Generating spice model of the Memristor.....	23
3.1.1 Simmons Tunnel Barrier Model	23
3.1.2 ThrEshold Adoptive Memristor Model.....	25

3.2 Section-2: Crossbar Array Architecture	28
3.3 Section-3: Feedback Based Non-destructive Read operation	
Circuit	33
CHAPTER 4 – Simulation and Result	36
4.1 Section-1: Analysis of a single Memristor.....	36
4.2 Section-2: 4×4 Non-destructive crossbar architecture of the	
Memristor	41
4.2.1 Writing to and Reading from.....	41
4.2.2 Feedback Circuit.....	43
CHAPTER 5 –Application.....	47
CHAPTER 6 –Conclusion and future scope.....	50
REFERENCES	51
VITA	54

LIST OF FIGURES

<u>FIGURE</u>	<u>PAGE</u>
Figure 1	2
Figure 2	9
Figure 3	10
Figure 4	11
Figure 5	13
Figure 6	15
Figure 7	16
Figure 8	17
Figure 9	18
Figure 10	19
Figure 11	20
Figure 12	21
Figure 13	22
Figure 14	24
Figure 15	27
Figure 16	28
Figure 17	29
Figure 18	31
Figure 19	32
Figure 20	33

Figure 21	34
Figure 22	35
Figure 23	36
Figure 24	38
Figure 25	39
Figure 26	40
Figure 27	42
Figure 28	43
Figure 29	44-45
Figure 30	46

CHAPTER 1

1.INTRODUCTION

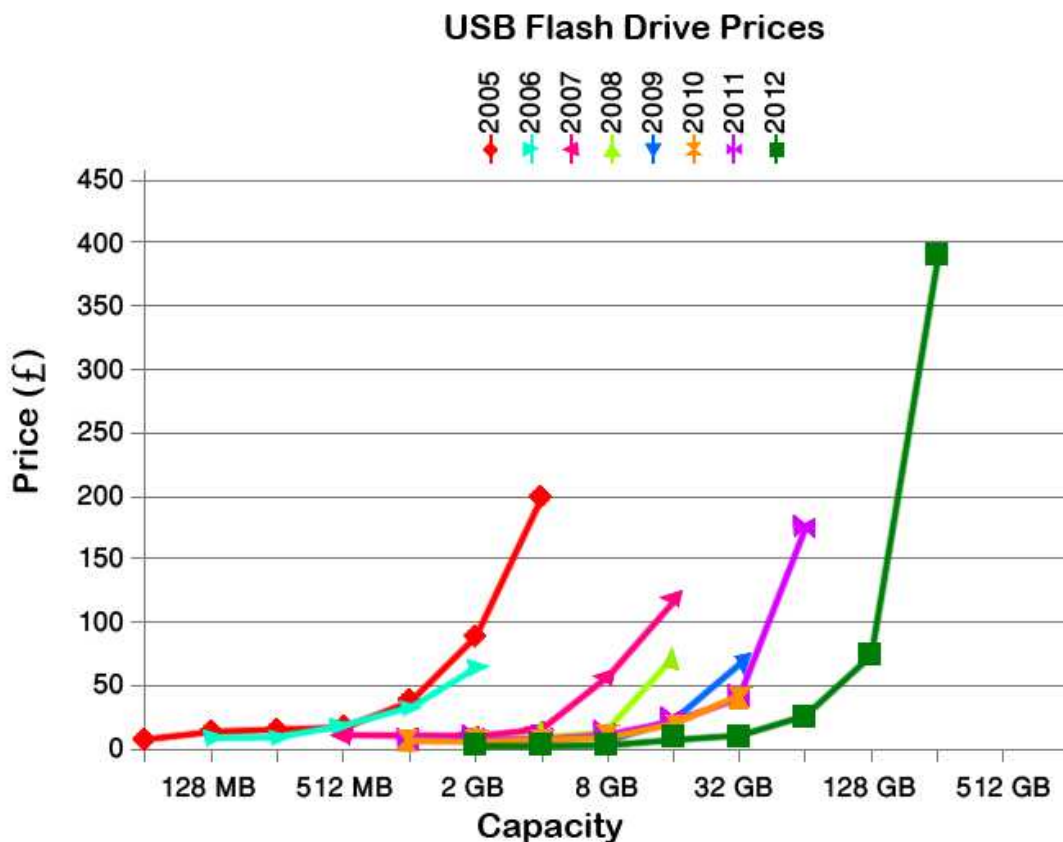
Hard disk, Floppy disc, Magnetic tape and Optical disk are just some examples of non-volatile Memory. Non-volatile Memory is a kind of memory that can retain the data even when there is no power supply. Flash memory which is a best example of NVMs first was introduced in 1984 by Dr. Masuoka as a developed version of EEPROM (Electrically Erasable Programmable Read Only Memory). The notable difference between EEPROM and flash is that in the EEPROM the device should be erased completely in order to be ready for write operation. Whereas in flash drives data should be written and read in blocks that are parts of the entire device. Recent Non-volatile memories are much faster compared to the first generation on NVM (floppy, Optical disc and etc.), however, they are still much slower than the technologies like ROM and SRAM which impede them to be used as a main memory in the computer architecture. Currently, the market demand of these Non-volatile Memories increased enormously and they became popular because of the portability and Non-volatility characteristics.

Recent advance in technologies such as creating high capacity storage computers and high definition television and cameras increased the demand of high capacity storage. In order to fulfil the needs and catching up with technology pace, companies are trying to increase the storage capacity. In 2005, Toshiba and Scan Disk developed a flash chip which was capable of storing 1 GB. In September 2005, Samsung Electronics developed the first 2GB flash drive. In March 2006, Samsung improved the

flash drive's capacity to 4GB. In September 2006, they increased the capacity of storage to 8GB by using 40nm manufacturing architecture [28].

Flash drives have made their way into much greater capacity (32GB and 64GB) today.

In order to attract the consumers, Price of the device is another challenging issue which has to be considered by manufacturing companies. As shown in figure (1), the price of flash drive decreased enormously during the time. Technology growth enabled the manufacturing companies to produce flash drives with much greater capacity and the same price as the previous flash drives.



All the price has checked at the middle of the year

Figure(1). Capacity versus Price of the flash drives from 2005 to 2012

The increasing demand for high speed, high capacity and low price non-volatile memory, attracted many researchers to work on developing memories in order to fulfil the market needs.

According to the Gordon Moore's law, the number of transistor per square inch on integrated circuits had doubled every year since the integrated circuits were invented. Moore predicted that this trend should continue for the foreseeable future [7]. However, John Gustafon, the chief product architect of AMD declared difficulty in transitioning from 28 nanometer chip to 20 nanometer which shows the beginning of Moore's Law's ending. Consumers always love smaller and faster devices meaning to increase density of the transistors at lower technology nodes. But these nodes faced the parasitic limitation in design and manufacturing which was not a problem in 130 nanometer technologies. As transistors shrink, interconnect lines between them become very thin, which causes a parasitic problem. On the other hand, by scaling the chip, parasitic capacitance and inductance will grow. Therefore, when we go beyond the 28 nanometer technology, these limitations become dominant and do not let us have an accurate device.

Aforementioned limitations forced researchers look for another alternative since they could not go beyond the current technology. Now they are looking for a substitute to replace memory element in order to shrink the memory chip and increase the capacity. Many replacements were introduced for current memory elements and one of them was Memristor (Memory Resistor) which was unutilized for many years.

1.1 Missing element:

Anyone who has a basic understanding of electronics should be familiar with the essential electronics' elements; the Capacitor (1745), the Inductor (1831) and the Resistor (1827). However, in 1971, Leon O Chua introduced the fourth essential two terminal passive element called Memristor (Memory-Based Resistor), which was the missing element at that time [3]. There are four fundamental electrical variables which are: Current (i), Voltage (v), Charge (q) and Flux (φ) . Therefore, the pair combination of these four variables would be six different formulas which are:

$$(v, i) \quad v = i * R$$

$$(\varphi, i) \quad \varphi = L * i$$

$$(q, i) \quad q(t) = \int_{-\infty}^t i(\tau) d(\tau)$$

$$(q, v) \quad q = c * v$$

$$(\varphi, v) \quad \varphi(t) = \int_{-\infty}^t v(\tau) d(\tau)$$

$$(\varphi, q) \quad ??$$

So, the Memristor with the Memristance M introduces a relation between flux linkage and charge density ($d\varphi = M dq$) . In this relation, if we consider the M as a constant, the device would perform as a simple resistance and there is no point of interest in this

device since we already have resistor element. But, if we have a nonlinear device in which the M is a Function of dq , the I-V characteristic of this device would be different comparing to the other passive elements. In fact, none of the other elements can show the properties of the Memristor which makes the Memristor unique. For the Current – Controlled Memristor a very basic mathematical form would be:

$$v = R(w, i) * i$$

While v is the voltage applied to the Memristor, R a resistance of the element which is the function of the current and position. Finally, i stands for the current through the device. Memristor can be considered as a switch from a high resistance to a low resistance. Below the threshold voltage, the resistance would be in ‘Off-state’ and for the voltages above the threshold; the switch will be in ‘On-state’ [2]. In 2008, a team at HP lab claimed that they found the Chua’s missing element by using a thin film of titanium dioxide [1]. In 2011, they claimed that the Memristor would be commercially available by the end of the 2013 which would be the best replacement for DRAM, SRAM and Flash. However, recently they postponed the Commercial availability to 2018.

After providing the first realization of Memristor by HP lab [2], many researchers tried to implement the device with different materials and structures to improve fundamental characteristics such as speed, dimension, power consumption and compatibility with CMOS architecture to make a suitable device for commercial purpose in the market [4-6].

1.2. Thesis Organization:

This work moves by giving an overview of the necessary background regarding the theories that are used in this work in chapter 2. Chapter 3 presents our methodology and introduces the idea of non-destructive crossbar architecture of Memristor. Chapter 4 includes the implementation and simulation result. Chapter 5 presents the applications of the Memristor in electrical circuits, and finally chapter 6 summarizes the paper and discusses the future directions this research may take.

CHAPTER 2

BACKGROUND

This chapter provides background information on the theories that form the basis of our methodology. First, we present a physical structure of the Memristor and we explain the theory behind this element. Then, we show the basic characteristics and behaviors of this device.

2.1. General Memristor:

General Memristor as proposed by HP lab in 2008[1], consists of the thin film with thickness D (10nm) which is sandwiched between two metal plates. As shown in figure (2), the device has two different areas with two different doping. The doped area (TiO_{2-x}), has a low resistance, and the undoped area (TiO_2), has a high resistance. The total resistance of the device would be the summation of the resistance of doped area and undoped area. The boundary between these two areas, and therefore the total resistance of the device depends on the position of w which can be controlled by applying a voltage with proper amplitude and pulse width. This applied voltage leads charge dopant to drift. In other words, when we apply a positive voltage through the Memristor, the current will pass through the device which leads to an increase of the resistance. By changing the direction of current, the resistance will decrease. It is obvious that passing current for a longer time will change the resistance more [2]. The

difference between the Memristor and other memory elements is that the Memristor is a variable resistor that can be changed by the direction and duration of applied voltage. Memristor can store a resistance instead of voltage which is the most significant difference between Memristor and other memory elements. As shown in figure (2), the device consists of two series resistors, the doped area with the width of (w) and the undoped area with the width of (D-w). Eq. (2), shows the total Memristance of the Memristor [1].

$$M(q) = R_{doped} + R_{undoped} \quad (1)$$

$$M(q) = \frac{w}{D} R_{on} + \left(1 - \frac{w}{D} R_{off}\right) \quad (2)$$

By considering linear ion drift in a uniform field with average ion mobility we will have Eq.(3).

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) \quad (3)$$

This leads to Eq.4:

$$w(t) = \mu_v \frac{R_{on}}{D} q(t) \quad (4)$$

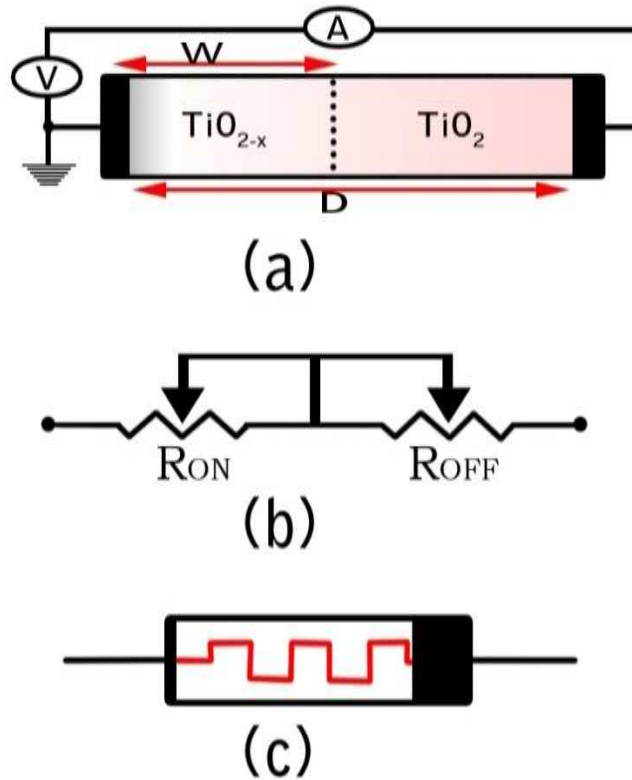
Eq.4 would be valid until the (w) is between zero and D. So, we have to multiply this equation with windows function in order to keep the boundary. When we apply large

voltage or when we apply voltage for a long time to the input of the device, the Memristor performs as a 'hard' switch. In this case (w) will approach the boundary (D) and the Memristor will be in the lowest state which represents the On-state.

By inserting this equation into Eq. (2) we will have:

$$M(q) = R_{off} \left(1 - \mu_v \frac{R_{on}}{D^2} q(t) \right) \quad (5)$$

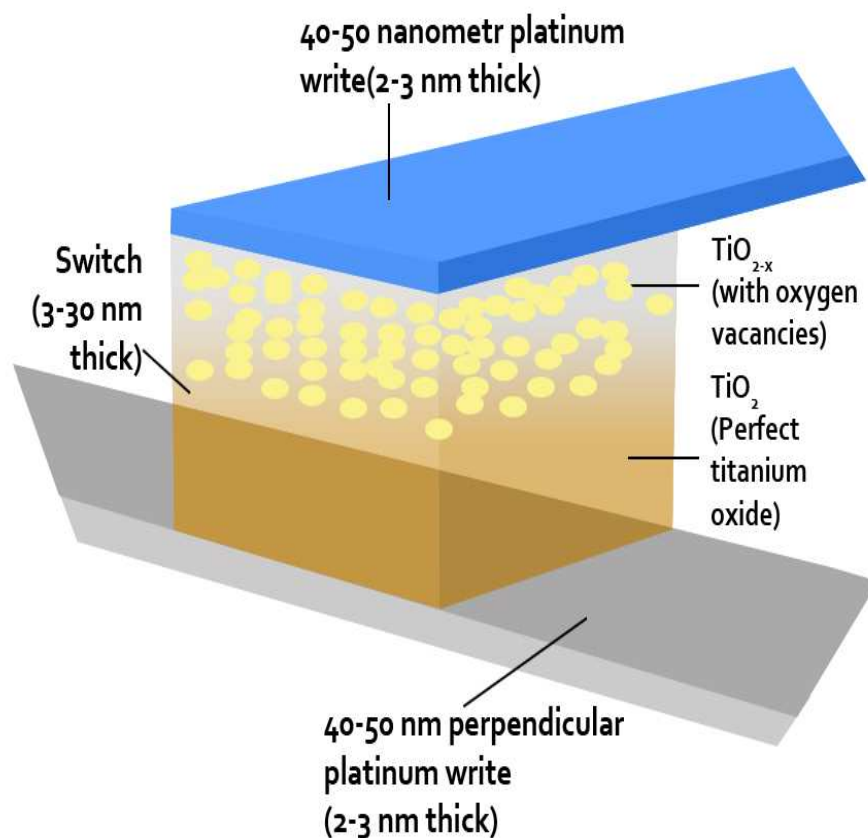
As shown in Eq. (5) the Memristance will be a function of charge, semiconductor thickness and mobility. By using a smaller semiconductor thickness and increasing the mobility (changing material), we can have a higher Memristance.



Figure(2).Physical structure of the Memristor.
 a.physical structure of the device with (w) as a width of doped region, and (D) as a width of entire device. b. circuit equivalent c. symbol of the single Memristor.

2.2. How Memristor works:

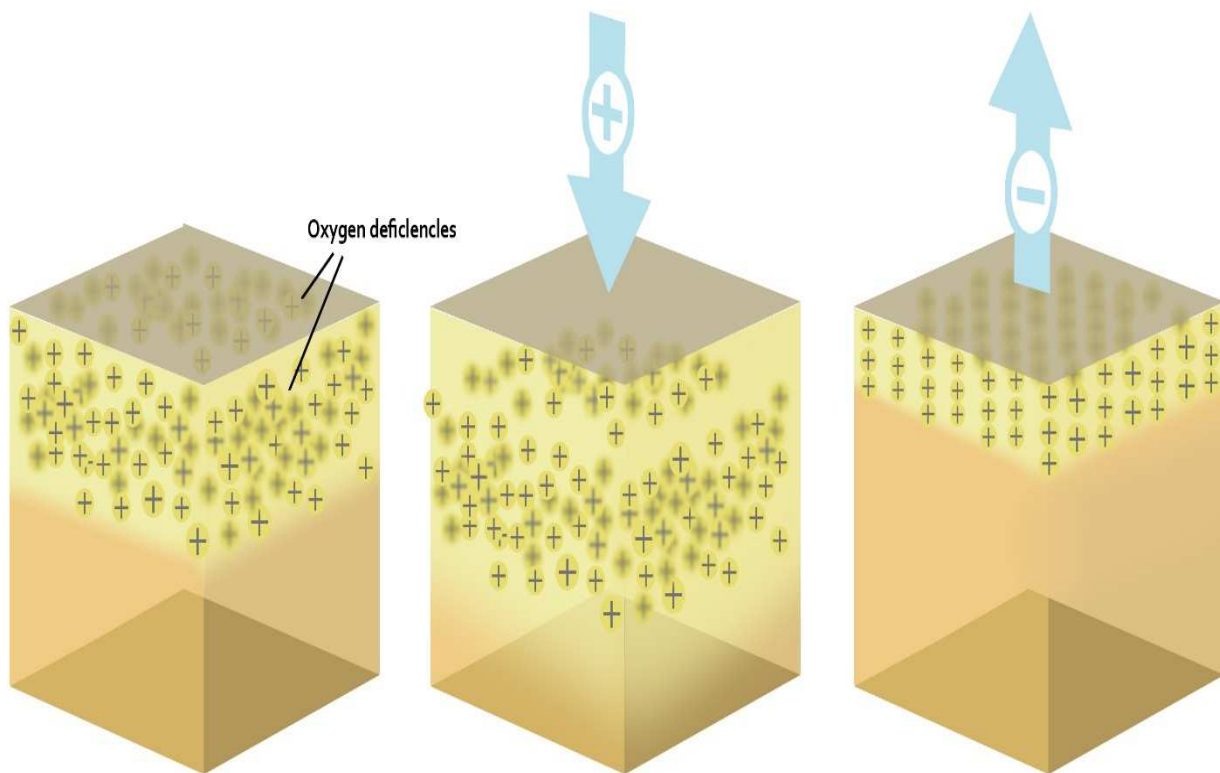
According to figure (3) which presents the HP lab model of the Memristor [9], the Memristor switch is a dioxide titanium cube (TiO_2) in two layers; the first (lower) layer consists of perfect TiO_2 with the ratio of 2:1 oxygen to titanium. The second layer is the TiO_{2-x} which lost 0.5 percent of its oxygen.



Figure(3). The Memristor structure

What makes this device unique is that the oxygen “bubble”, which scattered through the upper layer in doped area, will not move when the power supply is turned off. It means that the boundary between doped and undoped will freeze and memory can remember the last resistance.

As shown in figure (4), by applying positive voltage through the device, it repels the oxygen bubbles and pushes them to the lower side (undoped part). It means that the oxygen bubbles migrate from the doped area to undoped area; therefore, the boundary moves from doped area to undoped area. By applying the negative voltage, it attracts the oxygen bubbles so that the doped region will shrink and the boundary will go toward the doped region.



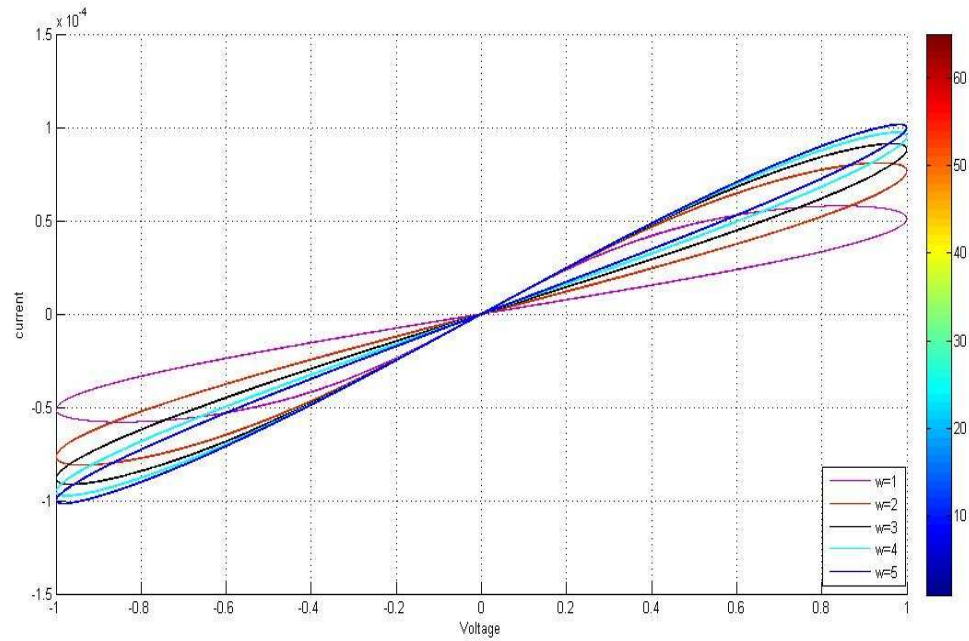
Figure(4) position of oxygen bubbles after applying voltage

2.3. Pinched Hysteresis:

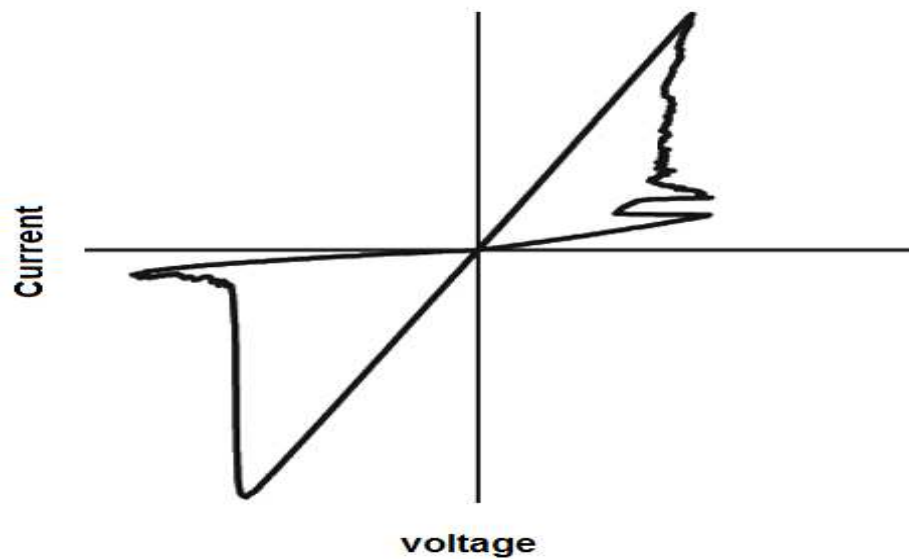
Resistor, capacitor, inductor and Memristor are all passive. The word 'passive' means that the device neither amplifies the voltage or current nor gives energy to the circuit. However, the transistor which is an 'active' element will amplify the current or voltage.

One of the characteristics of current controlled Memristor is the pinch hysteresis effect. By applying a sinusoidal voltage to the input ($v_0 \sin(\omega t)$), we have current through the device which creates the curve with the slope of resistivity. At very high frequency, the curve turns into a straight line which shows the characteristic of a linear resistor and it cannot be considered as a Memristor at all. The Memristor curve is 'pinched' because the voltage and current cross each other at the origin. The hysteresis effect makes the big difference between resistor and memory, whereas in resistor the relation between current and voltage is a straight line. The pinched hysteresis curve starts from the origin which shows that the Memristor will not store energy (just like the resistor) when the voltage and current are zero. However this is not true for a capacitor or inductor [8]. When we apply a sinusoidal input to the Memristor, we can have two different values for each voltage. It means that depending on the history of the Memristor, only one value of the current can be valid. As shown in figure (5.a), the hysteresis effect would be different for different frequencies and different amplitudes. It shows that if we increase the frequency, the device will approach a simple resistor. Figure (5.b) shows that by applying positive voltage to the input of the Memristor, the current will increase slowly. When the voltage increases, the current increases rapidly and the resistance starts dropping. This process will continue as the voltage reaches its

maximum value. After that, by decreasing the voltage the current will decrease slower than the voltage because there are charges flowing through the device and the resistance is still dropping [2].



Figure(5).a Pinched hysteresis effect at different frequencies based on Chua's equations.



Figure(5).b.Pinched hysteresis effect based on William observation on HP lab[9]

2.4. Different types of Memristors:

Before the first realization of a Memristor, many researchers declared that the memristor cannot be the fourth fundamental element and 'it is an obvious example of bad science' [9]. However, after proposing the first implementation of the Memristor by HP lab, researchers started to believe that this device can be functional and there are many characteristics of this element which are still unknown. As a result, many research areas opened about the Memristor and Memristivity. It is important to know the difference between Memristor and Memristivity since using different material to create a Memristor causes different behavior and characteristics (Memristivity). Different materials create different Memristors. So, Based on the application, we will use a certain type of material in order to adjust strengths and weaknesses. In general, all of the Memristors have hysteresis characteristics, but the shape of the hysteresis represents the Memristive properties. HP version of the Memristor is a general version of Memristor, however, after this invention many prototypes were introduced by manufacturing companies to use Memristor for different applications.

2.4.1. Titanium Dioxide Memristor:

a. Titanium Dioxide Memristor

Titanium Dioxide Memristor is a first version of the device that Stan Williams implemented in the HP lab [9]. He used a thin film of titanium dioxide which is

sandwiched between two metal layers. The top layer has some oxygen bubbles and the bottom layer is a pure titanium dioxide which performs as an insulator. By applying the input voltage, electrons migrate from the top layer to the bottom layer which leads to a change in the total resistance of the device.

b. Polymeric Memristor:

In July 2008, Victor Erokhin and M.P.Fontana [12] claimed that they found polymeric Memristor before the Titanium Dioxide version of Memristor. In this Memristor ions (cations and anions) are free to move in any direction in order to carry their charges. Ionic materials use dynamic doping to create hysteresis behavior. This Memristor is created by inserting a passive layer between active film and electrode [12]. The active film which is made by polymeric material forces the cations or anions from electrode toward the active film [10]. It is important to use super ionic material for the passive layer which allows us to use less input voltage in order to extract the ion and perform switching operation [11].

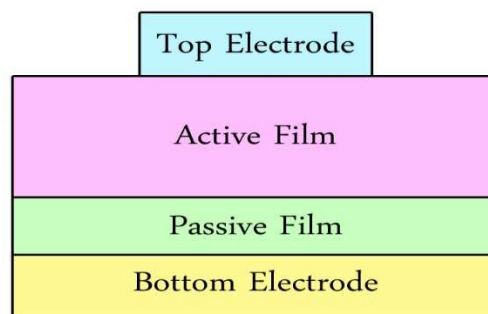
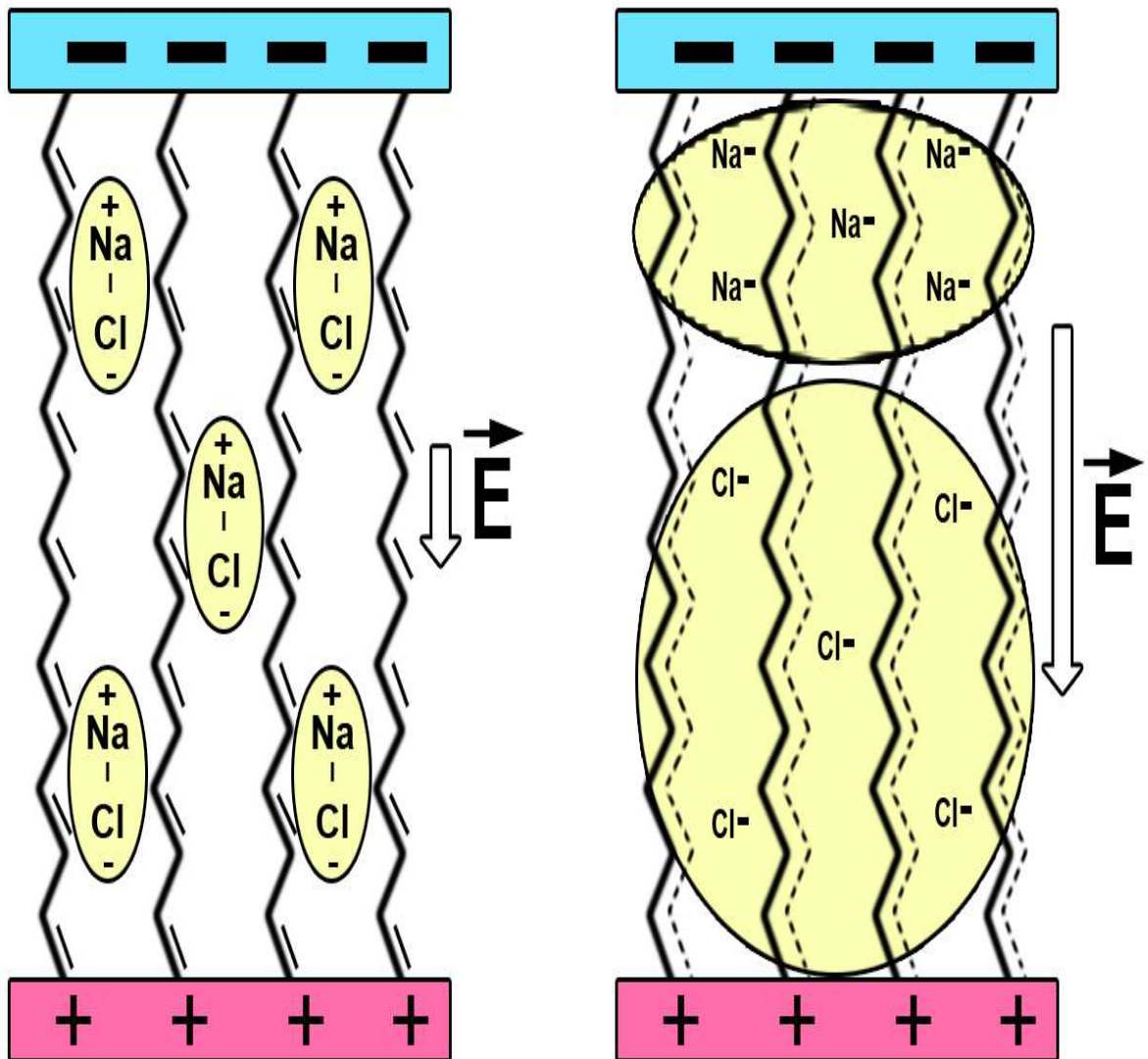


Figure (6). Structure of polymeric Memristor

The switching process has two steps: first, the forming process in which the ions extract from the electrode and migrate to the passive layer. The second step is the

formation of conductive bridge from the passive layer to the top electrode upon applied voltage. Figure (6) shows the single cell of polymeric Memristor with the position of active film, bottom electrode and passive layer. As shown in figure (7), positive ions are extracted from the bottom electrode layer and create the conductive bridge [10].



Figure(7). Ionic motion in the polymeric Memristor

By using a super ionic material for the passive layer, we can create pinched hysteresis characteristic when the voltages range is from -1 to 1 volt. Figure (8) shows the different regions of switching operation. Region (1) shows the 'off' state where the device is off and the resistance is high (about 20M ohm). When the input voltage reaches the threshold, the switch turns from 'off' state to 'on' state which has shown in region(2). In this region, the total resistance drops to 20k ohm. In region (3), we can see the memory effect of the device when the device is still in 'on' state. In region (4) the switch goes from 'on' state to the 'off' state and finally in region (5) the device will remain in 'off' state.

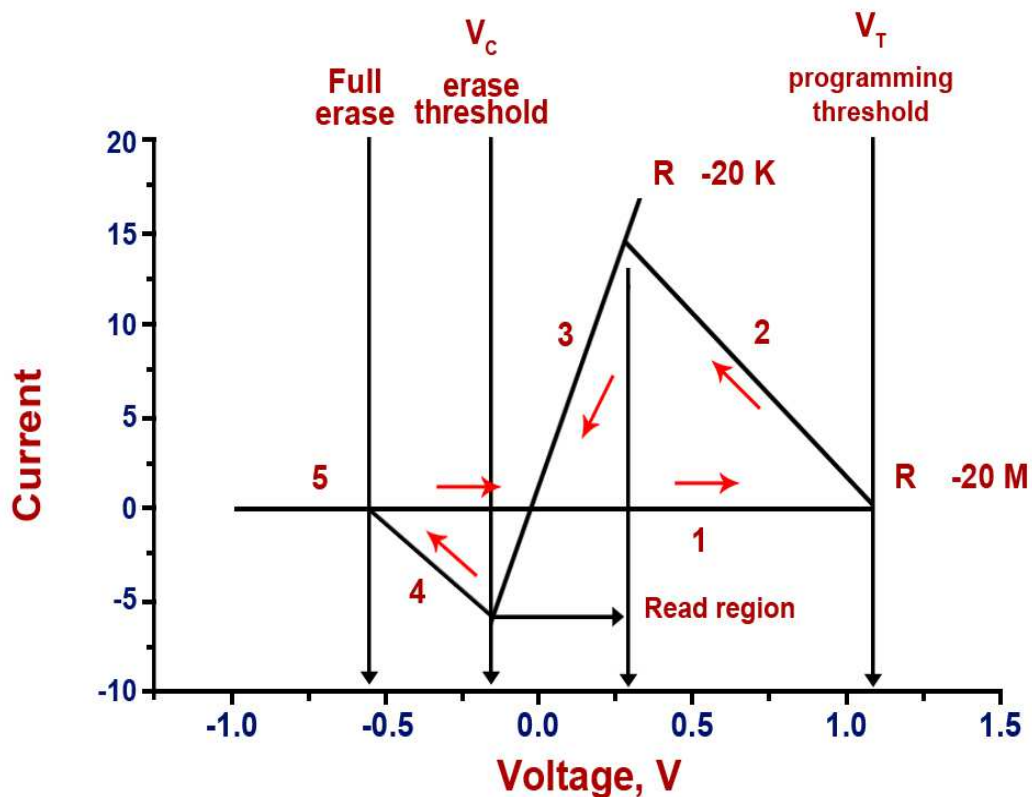


Figure (8) hysteresis effect in I-V characteristic of polymeric Memristor.

c. Manganite Memristive System:

In 2001, a group of researchers at University of Houston claimed that they found a new nonvolatile memory [13]. They studied bilayer oxide films based on manganite which described Memristive properties, however, they did not consider the term 'Memristor' for this device. In figure(9), graph represents the variable resistance based on the applied voltage pulses which is the same as the behavior of Titanium Dioxide Memristor introduced by Williams found in HP lab.

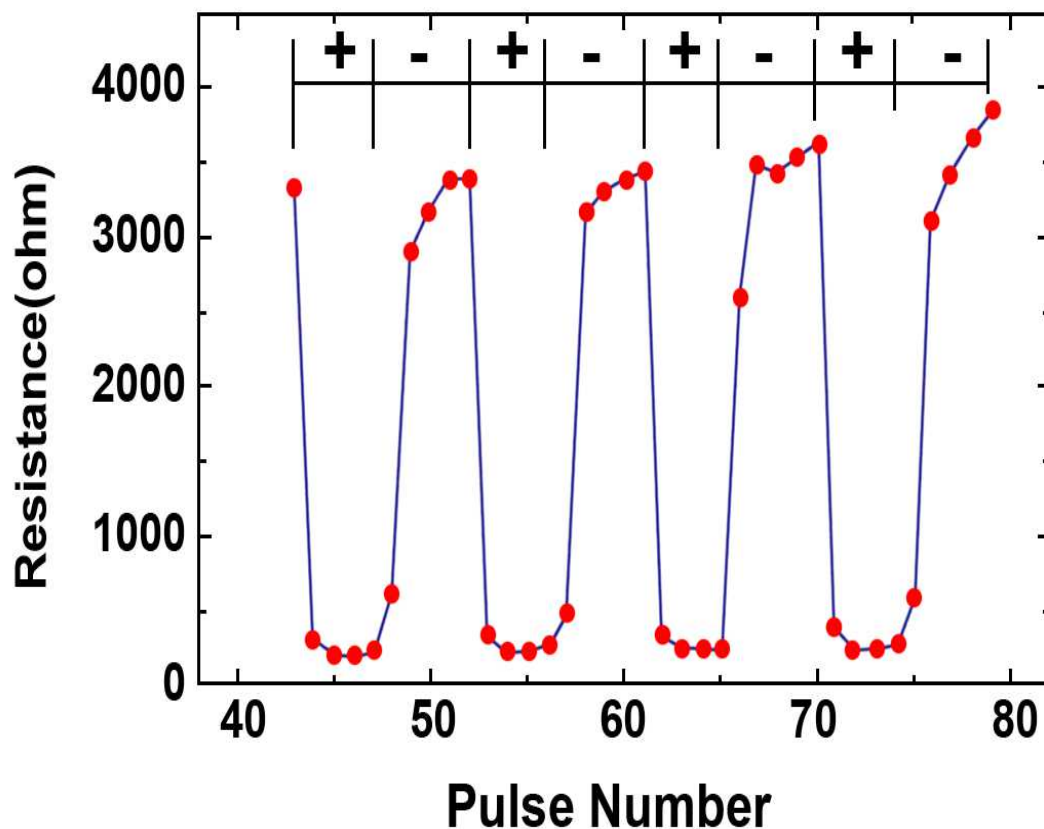


Figure (9). Non- volatile resistance Manganite film.

d. Resonant Tunneling Diode Memristor

In 1994, F.A.Bout and A.K. Rajagopal observed a 'bowtie' effect in the I-V characteristic of Resonant Tunneling Diode. They used a spacer layer between the source and drain with special doping in AlAs/GaAs/AlAs quantum-well diode in order to reach the 'bow tie ' I-V characteristic which was the same as the pinched hysteresis characteristic in Hp Memristor.[14]

2.4.2 Spin Memristive System:

In 2008, Yuriy V. Pershin proposed a completely different mechanism for Memristor. The mechanism of the Memristor is entirely based on electrons' degree of freedom [15]. They observed a Memristive behavior in the analysis of time dependent spin transport at the semiconductor junction.

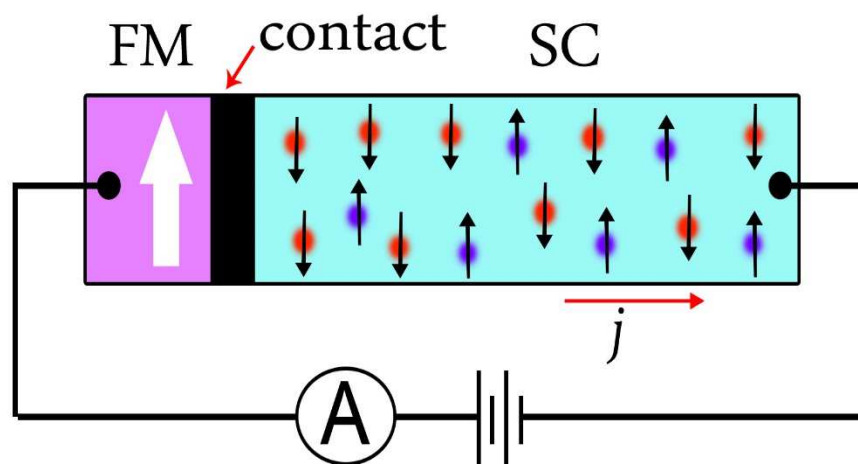


Figure (10). Spin Memristive system with semiconductor/ half metal junction

The device consists of semiconductor/half metal junction. The reason that they used half metal is because it acts as a perfect spin filter and that is more sensitive to the level of polarization. As shown in figure (10), the mechanism of the device is as the following: by applying the voltage, the half metal region will accept spin up electron and the current will flow through the system. On the other hand, spin down electrons cannot enter the half metal region and they will accumulate near the contact. By increasing the voltage, the current will increase, but at some point a cloud of spin down electrons will be created near the front of the contact.

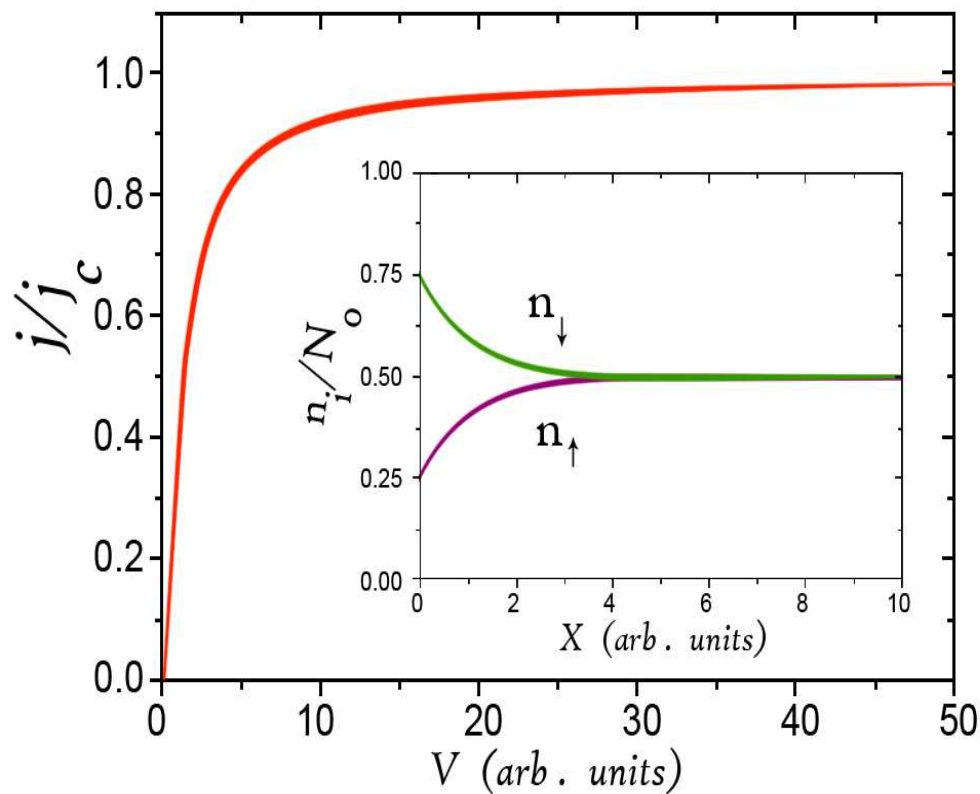


Figure (11). Flowing current through the half metal/semiconductor device

As shown in figure (11), at a certain point the density of spin up electrons becomes very negligible to increase the current flow through the device. As a result, by increasing the input voltage the current will be constant. According to this behaviour, this device has its potential to act as a Memristor. Figure (12) shows the frequency dependent AC response of the device which is similar to the pinch hysteresis effect of the Memristor proposed by HP lab.

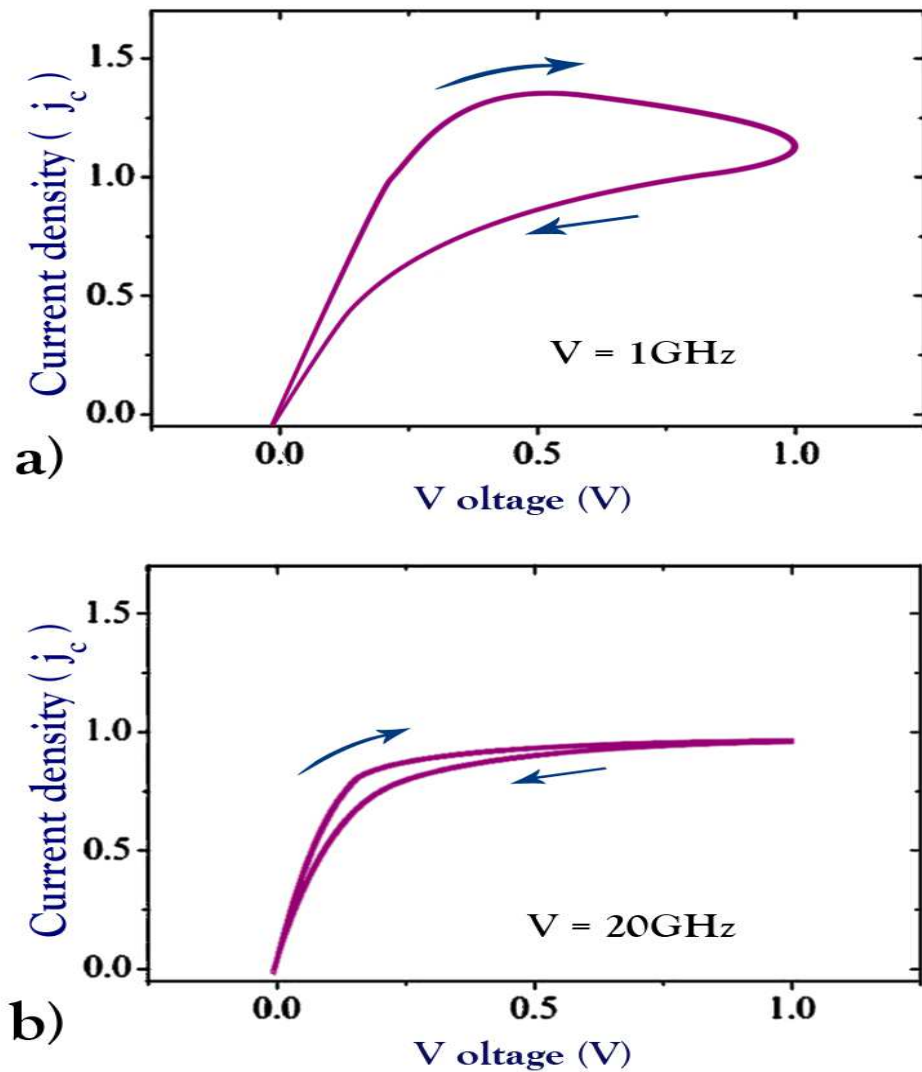
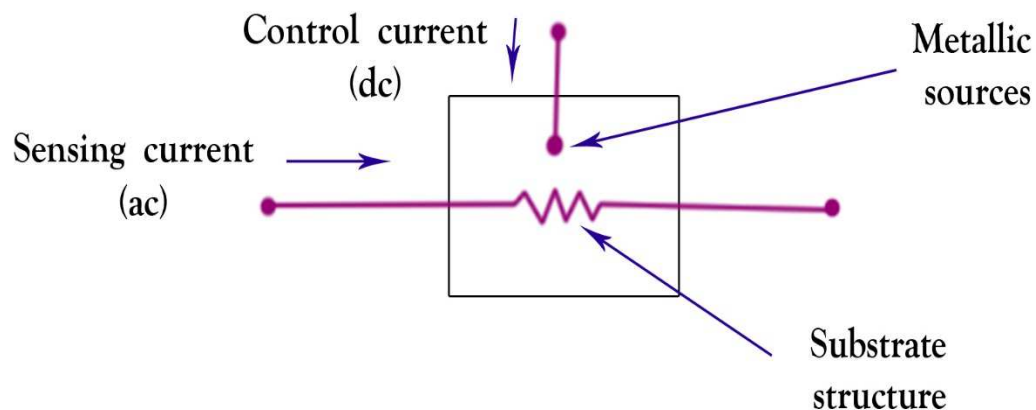


Figure (12). AC current/ voltage characteristic.

a. Input voltage with low frequency b. input voltage with low frequency

2.4.3. Three terminals Memistor:

In 1960, Bernard Widrow at Stanford University developed a new device called 'Memistor' (memory with resistor) to be used in neural network. The Memistor which is a three terminal version of Memristor, is able to store information and perform logic operations. In this three terminal element, the current flowing through the device is controllable by the time integral of the current [16]. As shown in figure (13), the Memistor consists of a source and the substrate which is the variable resistor. The substrate senses the AC current and the source controls the resistance of the substrate not by the DC current but by the integral of the source current. The Widrow's Memistor can be considered as a linear element since the resistance between two terminals of the substrate does not depend on the magnitude of input voltage. As a result, there will be no hysteresis effect on this device and this device cannot be considered as a Memristor. This element can be classified as an ad-hoc device [17].



Figure(13). Memistor's structure

CHAPTER 3

METHODOLOGY

In this chapter, we will explain a novel method for the read operation in the Memristor which allows the device to retain its data after read operation without information loss. In order to have a better understanding of the proposed method, we have divided this chapter into three sections: the first section introduces the spice model of the device used in our work. In the second section, we explain the crossbar architecture and consider the usage of it in the memoristor array which produces the crossbar Memristor. In the third section, we propose the feedback circuit for the crossbar Memristor which is the critical part of the crossbar Memristor in order to have a non-destructive read operation.

3.1 Section 1: Generating the spice model of Memristor:

3.1.1. Simmons Tunnel Barrier Model:

Linear [1] and non-linear [18][19] ion drift models of the Memristor are based on two different regions (doped and undoped) which are two resistors in series. However, these models were not accurate enough, so a more accurate model named Simmons Tunnel Barrier was proposed [20]. Figure (14) shows the structure of this model of Memristor.

This model has both asymmetric and nonlinear switching behavior because of exponential dependency on the ionized dopants movement (state variable). In this

model the derivative of the state variable would be the velocity of the ionized dopant.

Eq. 6 declares that the state variable is a function of current and (w) itself.

$$\frac{dw}{dt} = f(w, i)$$

(6)

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \sinh\left(\frac{i}{i_{off}}\right) \exp\left[-\exp\left(\frac{w - a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], & i > 0 \\ k_{on} \sinh\left(\frac{i}{i_{on}}\right) \exp\left[-\exp\left(\frac{w - a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], & i < 0 \end{cases} \quad (7)$$

(8)

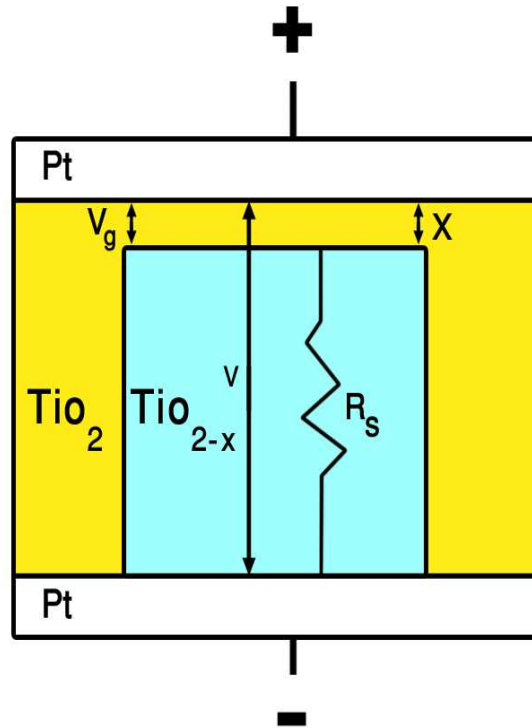


Figure (14) Structure of Simmons Tunneling Barrier model of the Memristor

In Eq.6 and Eq.7, parameters k_{off} and k_{on} define the magnitude of the state variable. i_{off} and i_{on} define the threshold current for 'on state ' and 'off state' . a_{off} and a_{on} define the upper and lower boundary of the variable state. So, there is no need to have a windows function to limit the state variable [21]. A spice model of Simmons Tunneling Barrier Memristor is provided in [22]

3.1.2. ThrEshold Adoptive Memristor Model (TEAM Model):

Simmons Tunneling Barrier model of the Memristor was the most accurate model of the Memristor however, the model was a little bit computationally complicated and also it did not define a clear relation between the voltage and the current [21]. So, there was a need to have a simplified model of the Memristor with an implicit relation between the voltage and the current. A complete spice model of the ThrEshold Adoptive Memristor is presented in [21].

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \left(\frac{i}{i_{off}} - 1 \right)^{a_{off}} f_{off}(x) & 0 < i_{off} < i \quad (9a) \\ 0 & i_{on} < i < i_{off} \quad (9b) \\ k_{on} \left(\frac{i}{i_{on}} - 1 \right)^{a_{on}} f_{on}(x) & i < i_{on} < 0 \quad (9c) \end{cases}$$

Eq.9 [21] defines the state variable relation for the TEAM model where the k_{off} , k_{on} , a_{off} and a_{on} are constant, i_{on} and i_{off} are threshold current which is similar to the

threshold voltage in MOS transistors. $f_{off}(x)$ and $f_{on}(x)$ work just like a window function to limit the state variable(x) between $[x_{on}, x_{off}]$.

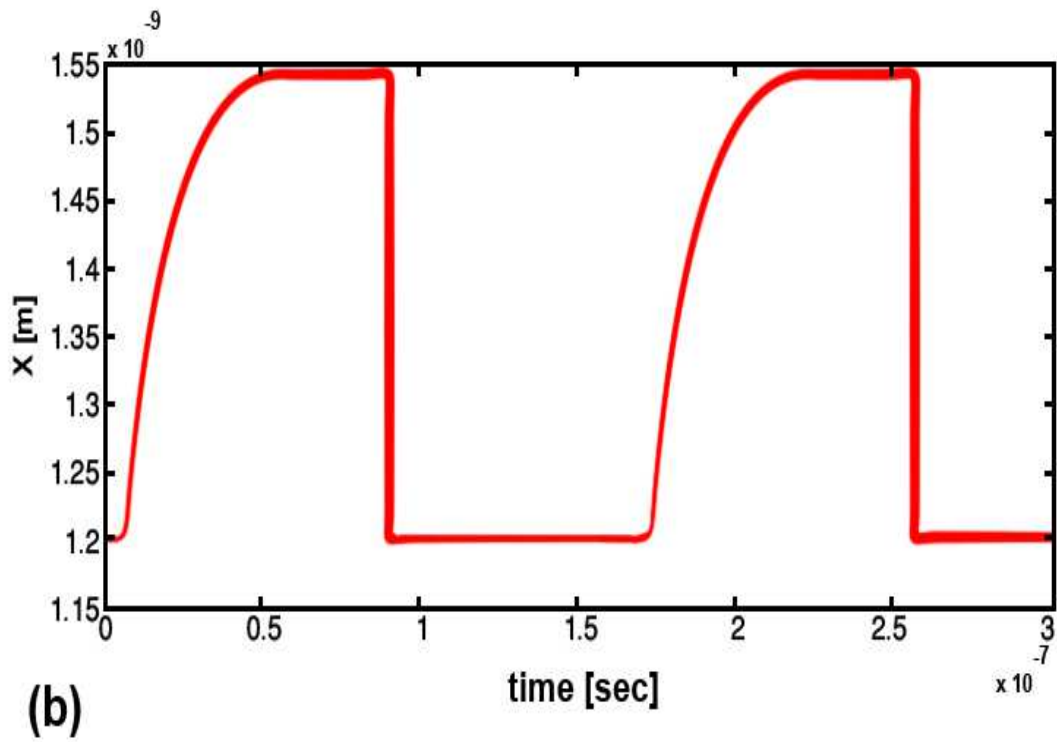
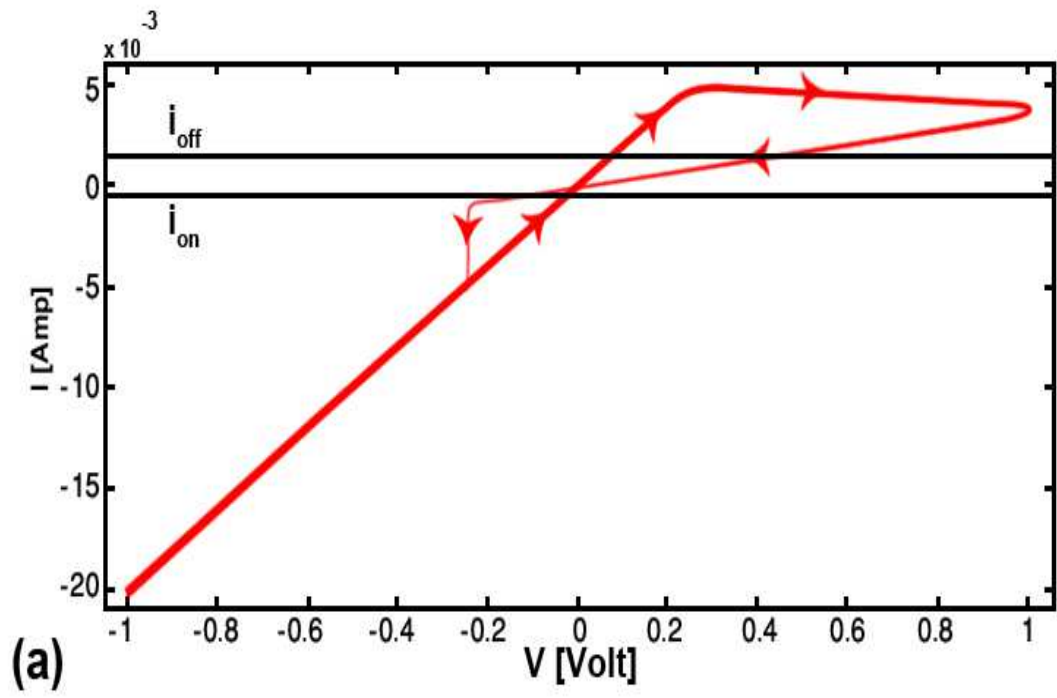
As mentioned, the Simmons Barrier model of the Memristor did not give us a clear relation between the voltage and the current, however, the TEAM defines the implicit relation between the voltage and the current which provided in Eq.10 [21].

$$v(t) = R_{on} e^{(\frac{\gamma}{x_{off}-x_{on}})(x-x_{on})} . i(t) \quad (10)$$

Where γ is the fitting parameter which defines the relation between R_{on}, R_{off} .

$$\frac{R_{off}}{R_{on}} = e^{\gamma} \quad (11)$$

Based on the Eq.10, every change in the tunnel barrier width causes a change in the total resistance exponentially. Figure (15) shows the hysteresis effect of TEAM model which is almost similar to the HP Memristor.



Figure(15) a. I_V characteristics of TEAM model Memristor

b. position of boundary in the device

3.1.2 Section 2: Crossbar array design:

In order to have a high density memory chip, we have to use the crossbar architecture which let us enhance the capacity by saving the area. Based on the desired density, the crossbar architecture consists of rows and columns which are the horizontal and vertical nanowires. These horizontal and vertical nanowires meet each other at the cross points. By using the Memristor at each and every cross point, we can control each cell of the memory. In order to control a specific cell we have to activate the related rows and columns. For instance, as shown in figure (16), if we want to activate the memory cell which is located at the cross point of b_1 and a_1 , we should apply an appropriate voltage to row a_1 and column b_1 .

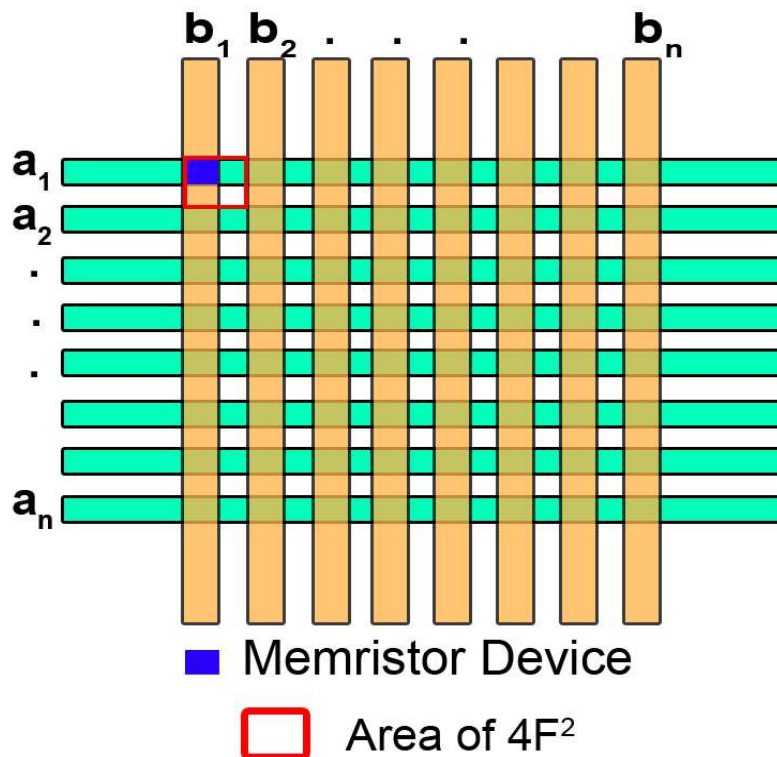
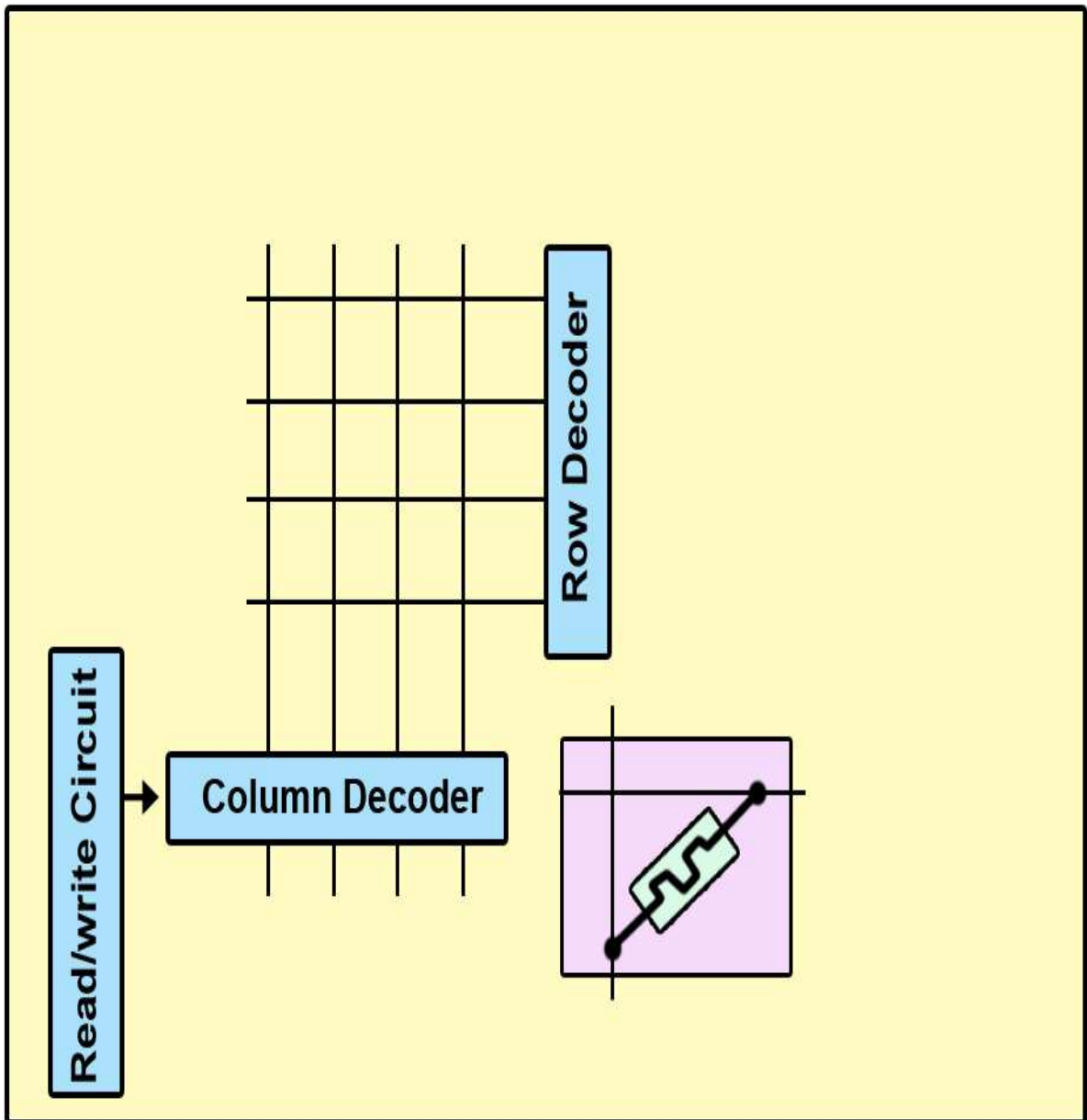
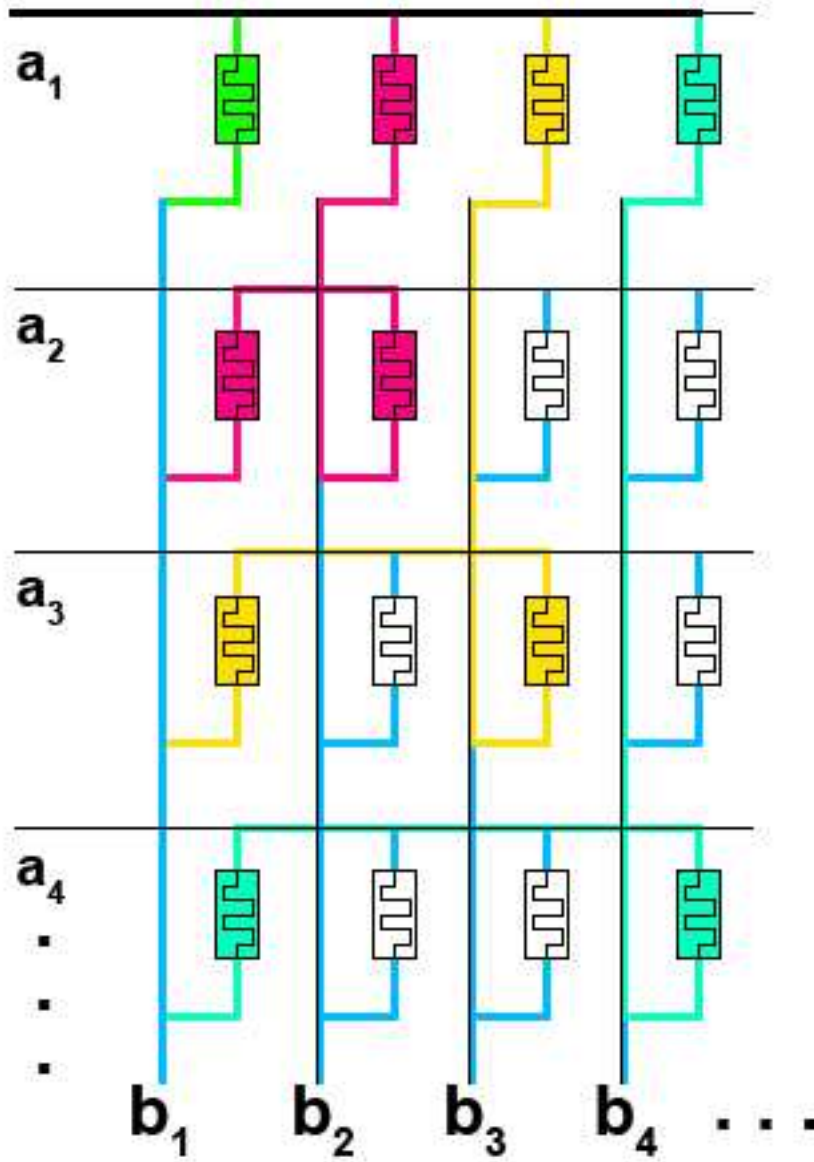


Figure (16) The crossbar architecture



Figure(17) Full circuit of the memory array.

As shown in figure (17), the Memristor array generally consists of a row decoder, a column decoder and a Read/Write control. Row decoder typically controls the row that should be selected for read and write operation and column decoder selects the related column in order to activate a specific cell. In this architecture as explained before, the Memristors are placed at each and every cross point and are set to the high resistivity (R_{off}). In write operation, the row decoder selects the related row, the column decoder chooses the related column and finally the Read/Write prepares the array to be written by the input voltage. Write operation changes the resistance of the selected cell from R_{off} to R_{on} . It means that whenever we write on each cell, we change the resistivity from high to low. Even though the write operation is pretty simple and clear, the read operation is a little bit challenging. In read operation, we are trying to sense the Memristive difference among the cells. As a matter of fact, this is a process of resistance comparison. In the Memristor, the read operation can also be destructive where it can change the resistance of the intended cell after each operation. Another challenging issue in cross bar architecture is 'Sneak Paths' which are the undesired current paths that enable the other Memristors parallel to the intended one [23]. Figure (18) shows the undesired current path during the read operation. For instance, consider the case in which we want to activate the green cell. To do this, we need to enable row a1 and column b1. By activating the a1 and b1, other Memristors which are shown by red, yellow and blue will also be activated.



Figure(18). Sneak path in crossbar array

To avoid this undesired current path, we can use a switch before all of the Memristors to prevent the current flowing to the undesired devices. One possible solution to solve this problem is 1T/1M structure which is proposed in [24]. This structure limits the power consumption by removing all of the undesired paths and decreasing the read failures.

However, it will increase the area of the memory chip where the areal density is not related to the memory cell anymore and it limits to the area of the transistor. Figure(19) show the structure of 1T/1M crossbar architecture.

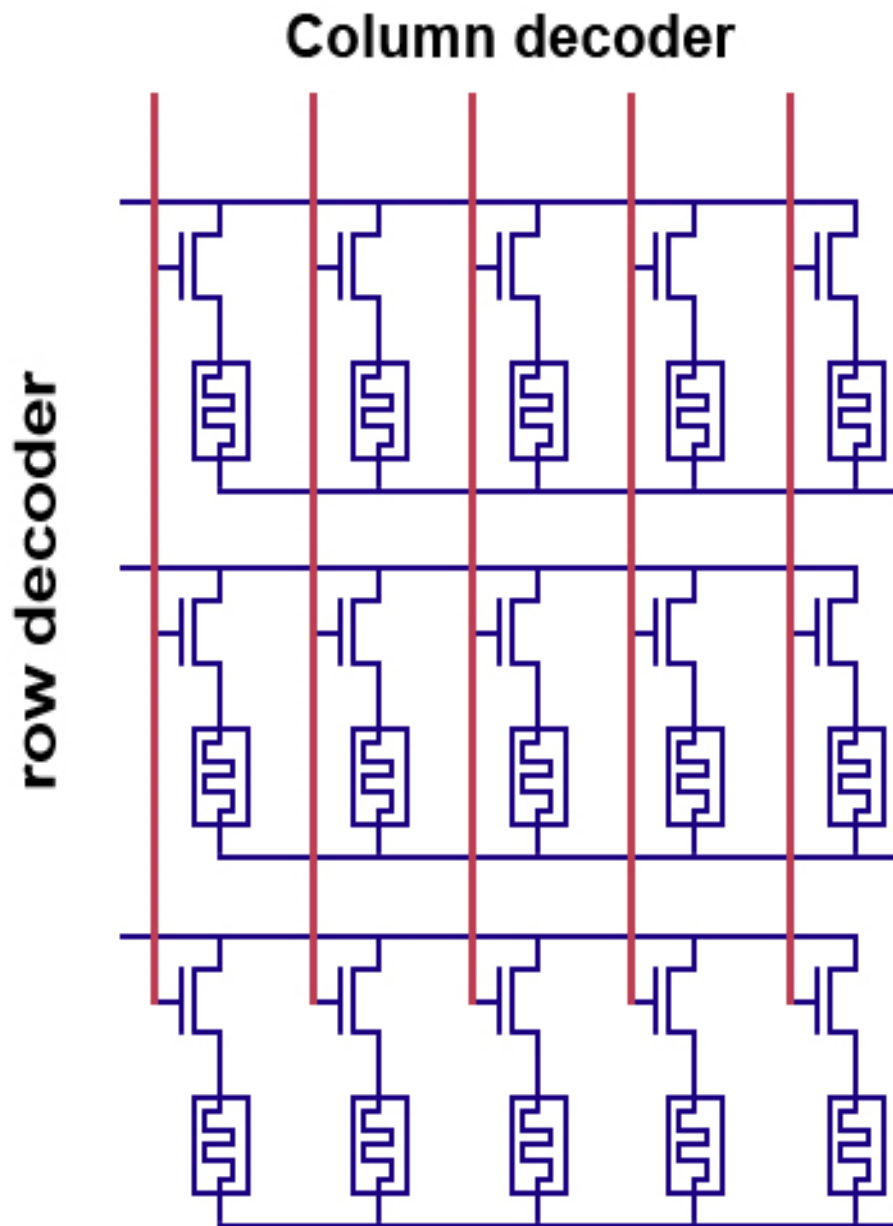


Figure (19). Structure of 1T/1M Memristor crossbar array

3.1.3. Feedback based non-destructive read operation circuit:

As we explained before, the resistance of the Memristor depends on the input voltage magnitude and the pulse width. By applying a wider voltage as an input, we can store more resistance. But this relation is not linear which goes back to the non-linearity feature of the device. This feature enables us to have a multi stage resistance which means storing multi data in a single cell.

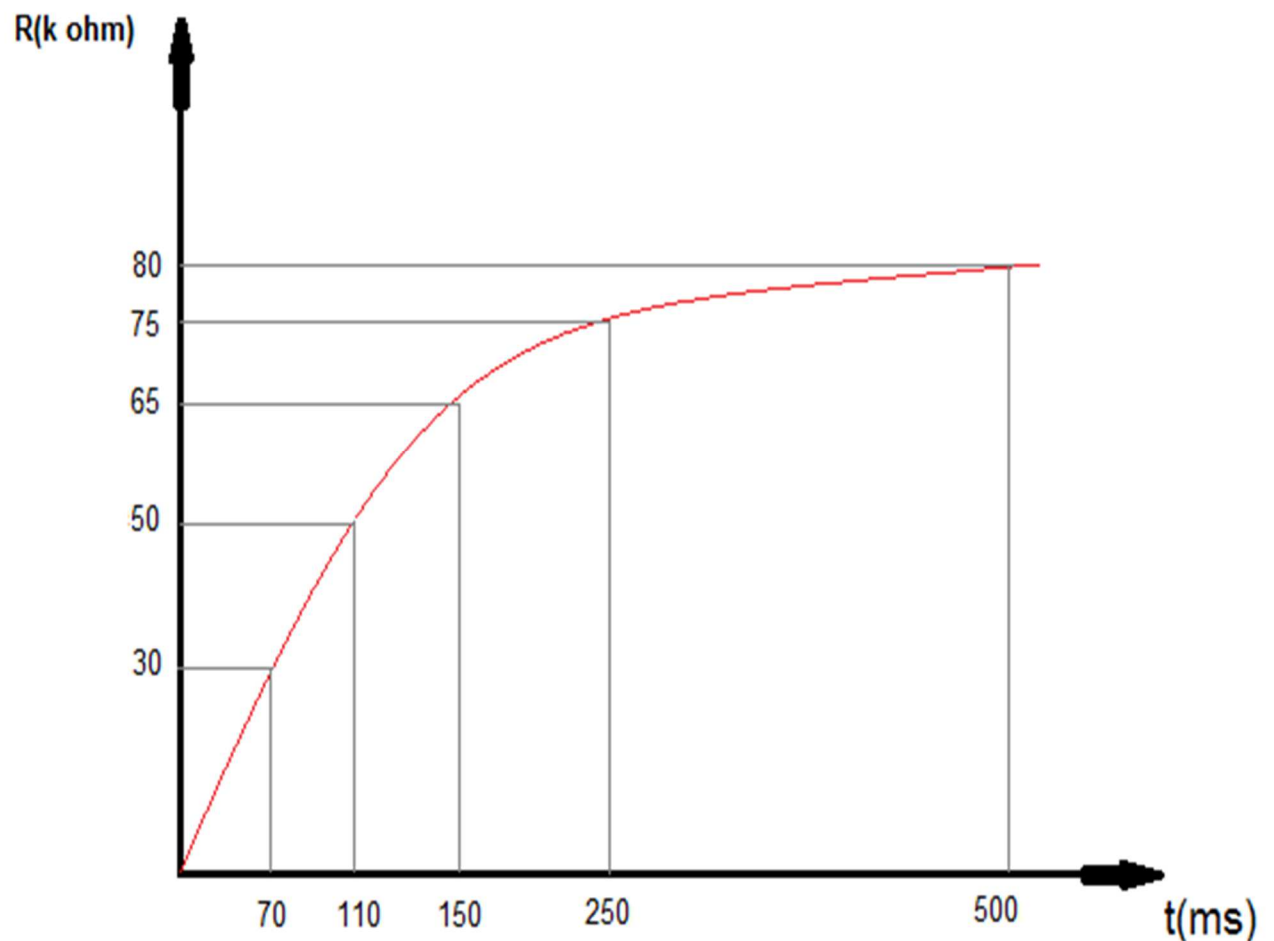


Figure (20). The effect of the pulse width on the resistance

As shown in figure (20), which is the result of our simulation in 90nm technology, by applying a pulse with 1 volt magnitude and 70ms pulse width, the resistance of the memristor will be 30kohm. As the pulse gets wider, the resistance increases nonlinearly which is the interesting feature of the Memristor.

In this section which is the main section of our work, we propose our novel design of a non-destructive circuit to correct a read operation and decrease the read failures. As we explained before, after each read operation, the voltage dropped at the Memristor changes. Therefore, the total resistance of the Memristor changes which translates as a loss of information. In order to retain the data and avoid read failure, we need to refresh the input voltage after each read operation. In our work, we proposed a feedback circuit to retrieve the information after each read operation.

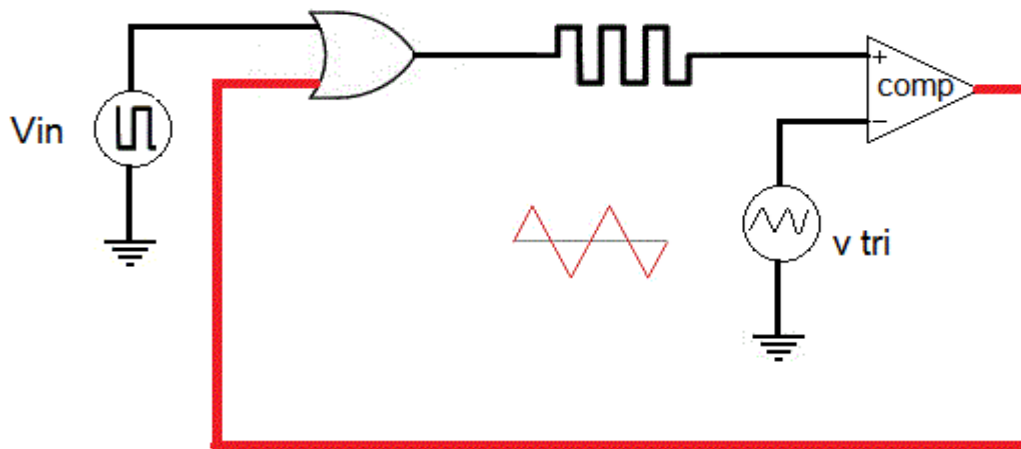


Figure (21). Proposed feedback path for the crossbar array.

As shown in figure (21), at the very first time when we apply the voltage to the input of the Memristor, the resistance of the device will increase exponentially (Based on TEAM

model). So, this voltage will be compared with the triangle wave and based on the comparison the pulse will be created. This pulse goes to the input of the Memristance to retrieve the destructed value. By this feedback path which is shown in red in figure (21), the Memristor can reach its previous value after destructive read operation. Figure (22) shows the comparison method and the process of producing the output pulse related to the voltage dropped at the output of the Memristor. As shown, if the voltage is high, the output pulse will be wider and vice versa. So, whenever the output of the comparator is one, it has two meanings: first the Memristor is in 'on state' and second the pulse is related to the amount of the resistance. By this method, not only we could read the data but also pass it to the output of the comparator. This outcome pulse will go to the input of the Memristor in order to recreate the data.

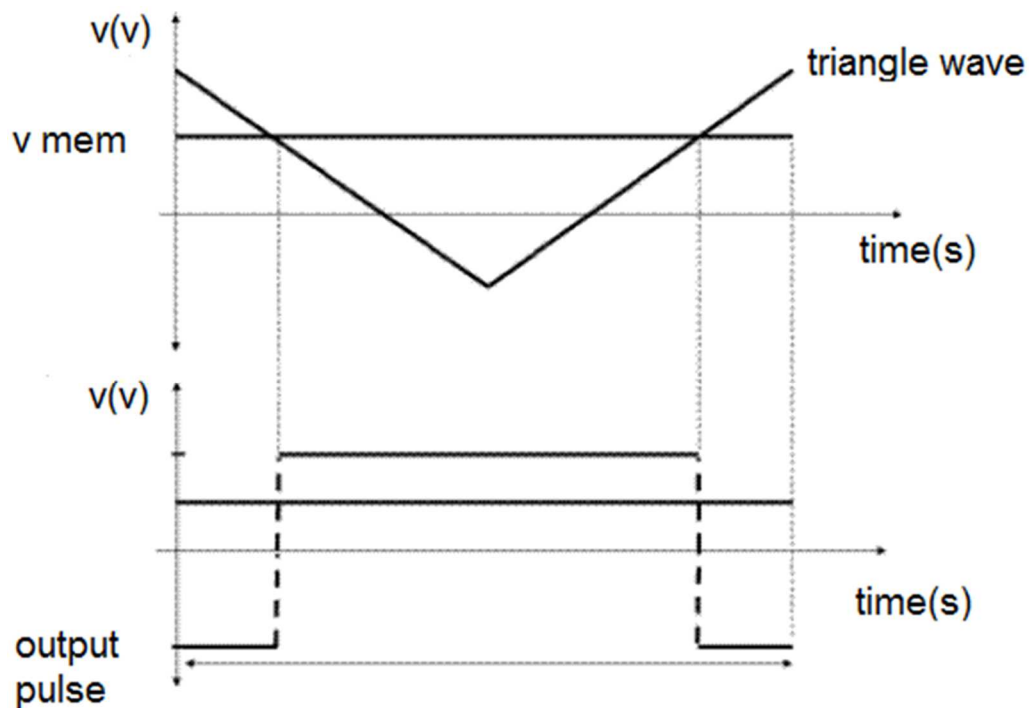


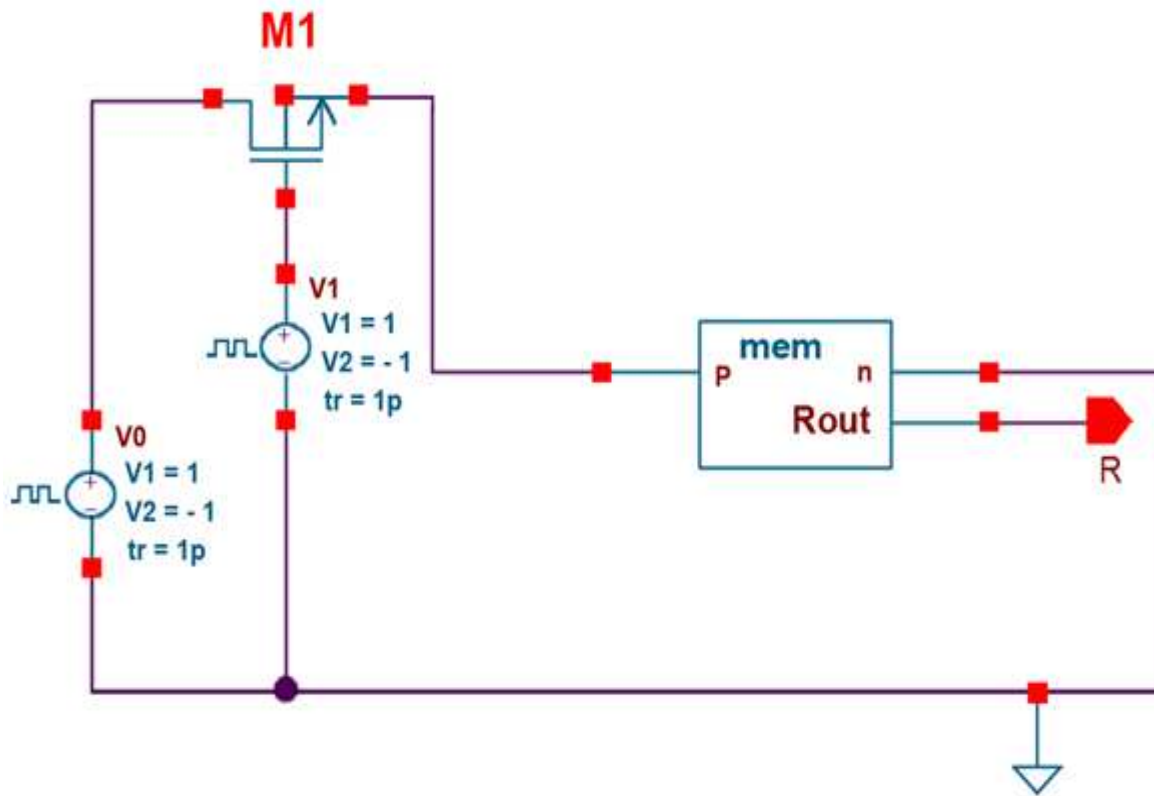
Figure (22). Comparison method in feedback circuit.

CHAPTER 4

SIMULATION AND RESULT

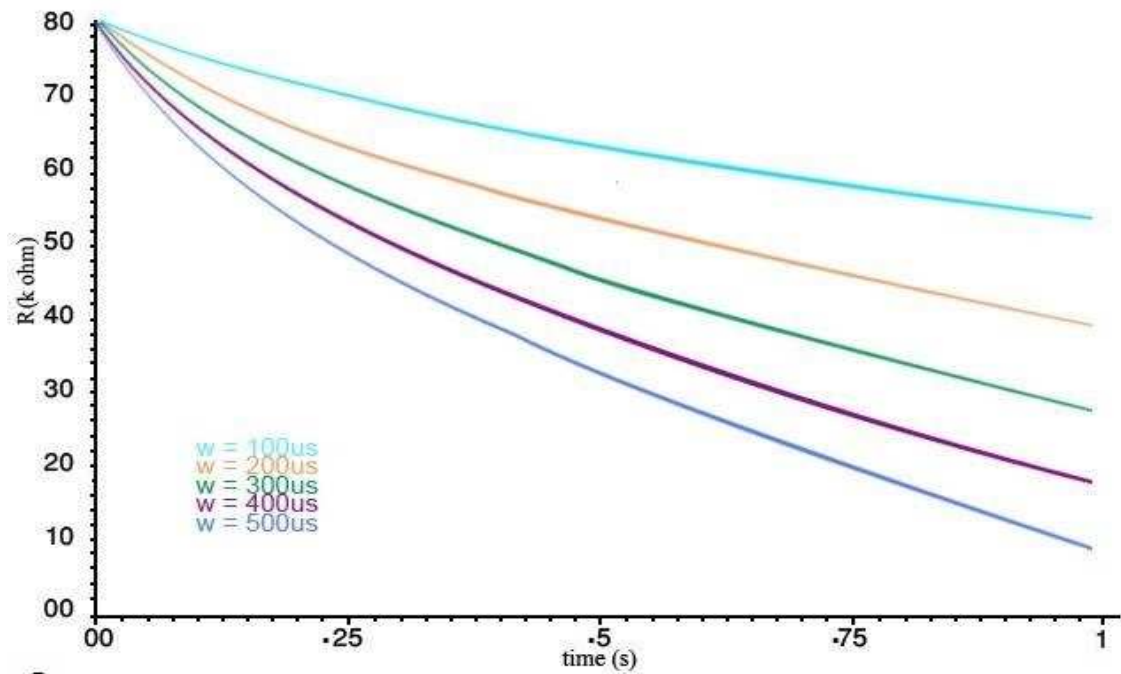
The first part of this chapter provides the simulation result for the single Memristor. The second part shows the simulation result of the feedback circuit in the Memristor crossbar array.

4.1. Section one: analysis of single memristor:

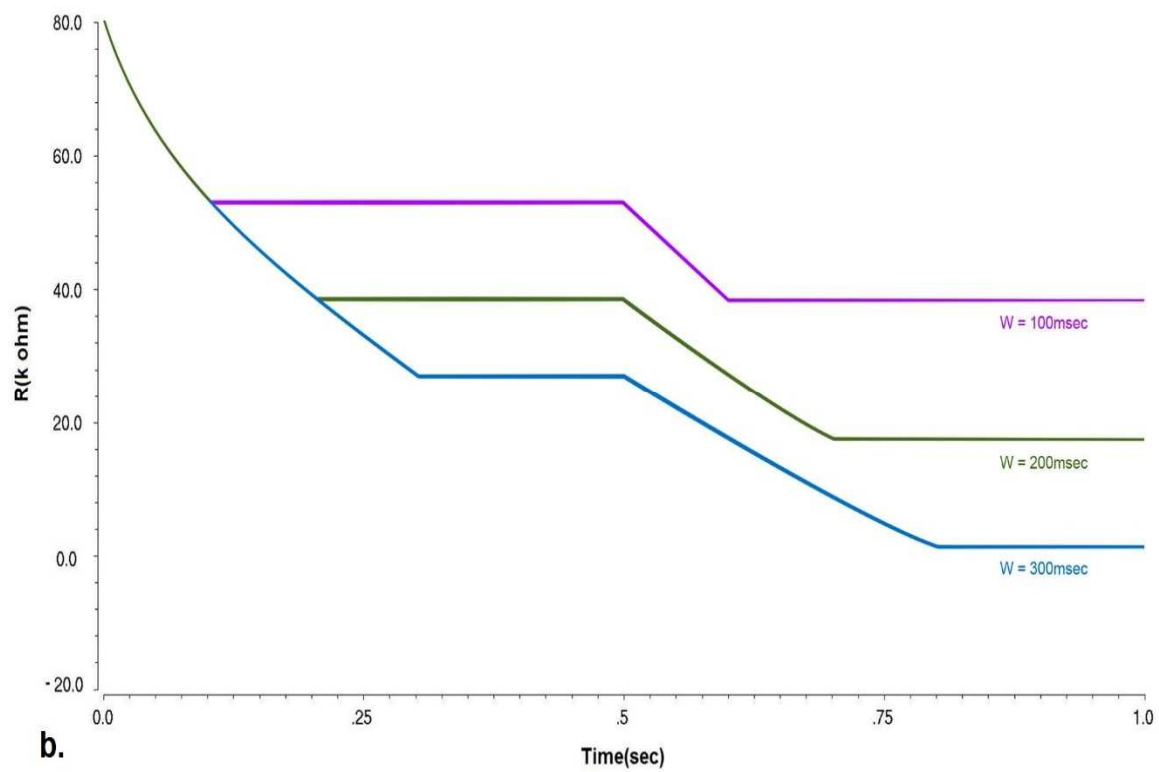


Figure(23) single Memristor configuration

In figure (23), we used a single Memristor as a single memory cell to analyze the behavior of the element under applying the input voltage. In the single float Memristor, before applying any voltage, the resistance is equal to R_{off} which is around 80 k Ω . When we apply a positive voltage to the Memristor, the resistance decreases exponentially approaching R_{on} which is 5 k Ω in our model. On the other hand, by applying a negative voltage to the Memristor, the resistance will go back to R_{off} (according to the hysteresis effect). As we explained in figure (20), the resistance of the Memristor greatly depends on the pulse width. By increasing the width, the Memristor will reach its upper band and lower band (R_{on} and R_{off}) faster. In comparison, by decreasing the width, the resistance changes slower because each pulse has less effect on changing the resistance. We can use this feature to store different data in a single cell. So, by applying various pulse widths, we can have different resistors. As shown in figure (24), different pulses can make different resistances. In the initial state, all of the Memristors are in 'off-state' which are around 80k ohm. By applying the positive voltage, the resistance is going to decrease exponentially. By disconnecting the input voltage the Memristor will keep its resistance which is the Memristivity feature of the device. Whenever we change the polarity of the input voltage (negative voltage), the Memristor tends to return to its initial value which is R_{off} . As a result, for the write operation we have to apply a positive voltage with different widths to store different values. On the other hand, to erase each cell we have to apply negative voltage to change the Resistance back to its initial value. The speed of the erasing depends on width and amplitude of the applied negative voltage.



a.



b.

Figure (24). Memristor's response to different input pulses in range of: a. micro second b. millisecond.

As mentioned before, applying various voltages to the Memristor leads to store different values on the Memristor. In figure (25), we applied five different pulses to the input in order to see the Memristor response to these different values. As shown in figure (26), for the thin pulse which was 100m sec, the resistance decreased to 55k ohm. For a wider pulse (200msec), which is shown in yellow, the resistance decreased to almost 40k ohm.

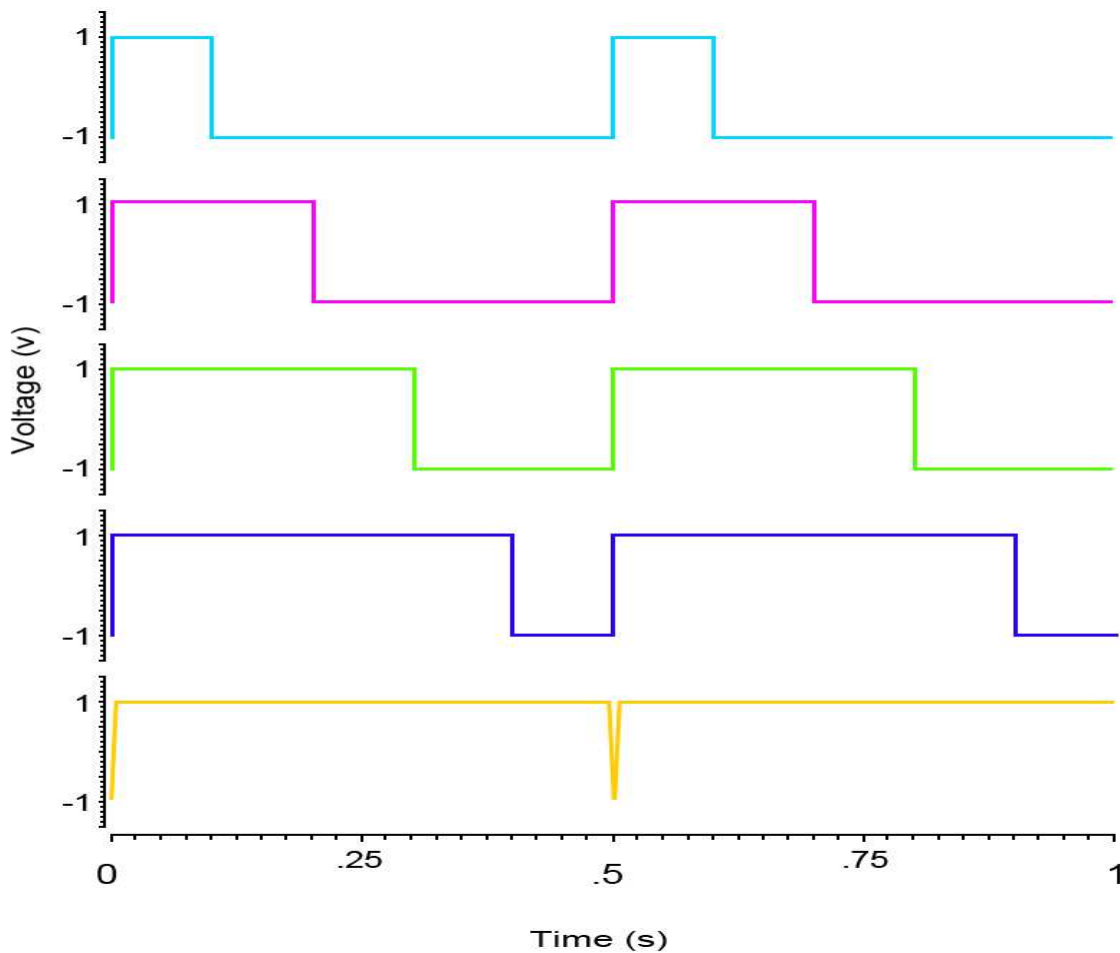


Figure (25) applying different pulses to the input of the Memristor (we also applied negative pulse in order to show the erase operation)

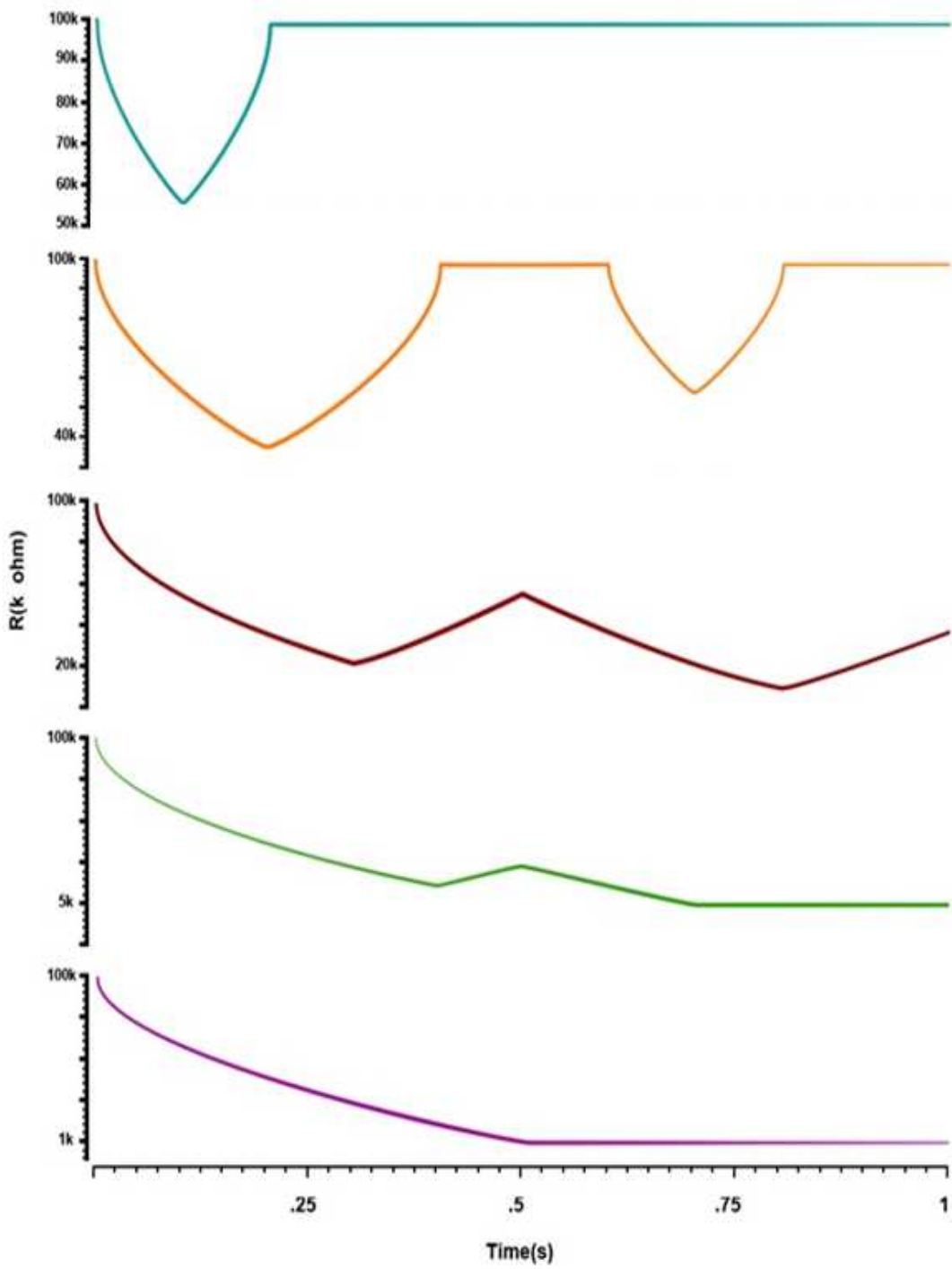


Figure (26). Writing different values on the Memristor.

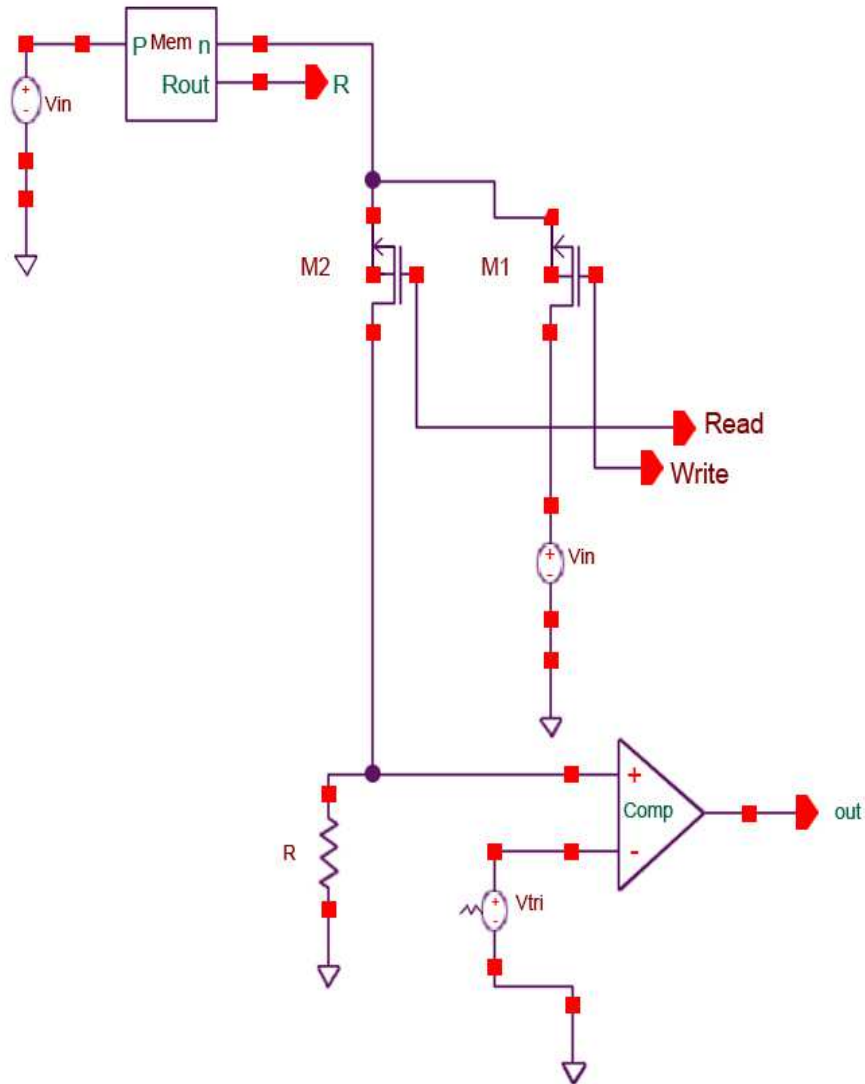
For the wider pulse (300msec which is shown in figure (25) in green), the resistor decreased to 20k ohm, but the negative voltage pulse was not wide enough to make the resistor back to its initial value. So, after applying the next positive voltage, the resistance starts decreasing from its previous point. Same thing will happen for the 400 msec pulse. For the constant voltage, the resistor will go all the way down to reach R_{on} value which is 1k ohm.

4.2. 4×4 non-destructive crossbar architecture of the Memristor:

4.2.1. Writing to and Reading from:

As shown in figure (27), reading and writing operations are controlled by the Read/Write Enable circuit. First, let's consider the writing operation. In order to write data, we have to apply a positive voltage to select a desired row. According to the hysteresis effect, the voltage at the Memristor starts to grow, but this voltage would not be enough to write data. Therefore, in order to make a bigger potential difference, we need to enable the gate of the M1 and apply a negative voltage to the other pin of the Memristor. In this case, by enabling the write operation, the voltage will be applied to the related column and by applying the positive voltage to the related row, we can write in a specific cell. In the reading operation, by activating the M2, the voltage of the related column will drop at the positive pin of the comparator and it goes for comparison with the triangle wave. The output of the comparator will be either zero or a pulse related to the resistivity of the desired column. When all of the Memristors are 'off', then the voltage dropped at the comparator will be zero. This voltage will be compared with

the triangle wave and the result will be zero because the triangle wave is greater than the voltage dropped at the Memristor. The output of the comparator will apply to the OR gate and finally it goes to the related Memristor to retrieve a related resistance value.



Figure(27). Reading and writing operation in crossbar array

By changing the voltage level of the triangle wave, we can adjust the output of the comparator in order to calibrate the resistance of the Memristor.

4.2.2. Feedback circuit:

In figure (28) we added the feedback circuit which consists of the transistor M3 and the OR gate. Gates of M1 and M3 tie together in order to be activated for read operation. Whenever the read operation is enabled by M1, the comparator produces the related pulse and passes it to the OR gate. By applying the output of OR gate to the Memristor, the element can retrieve its previous value based on the input voltage.

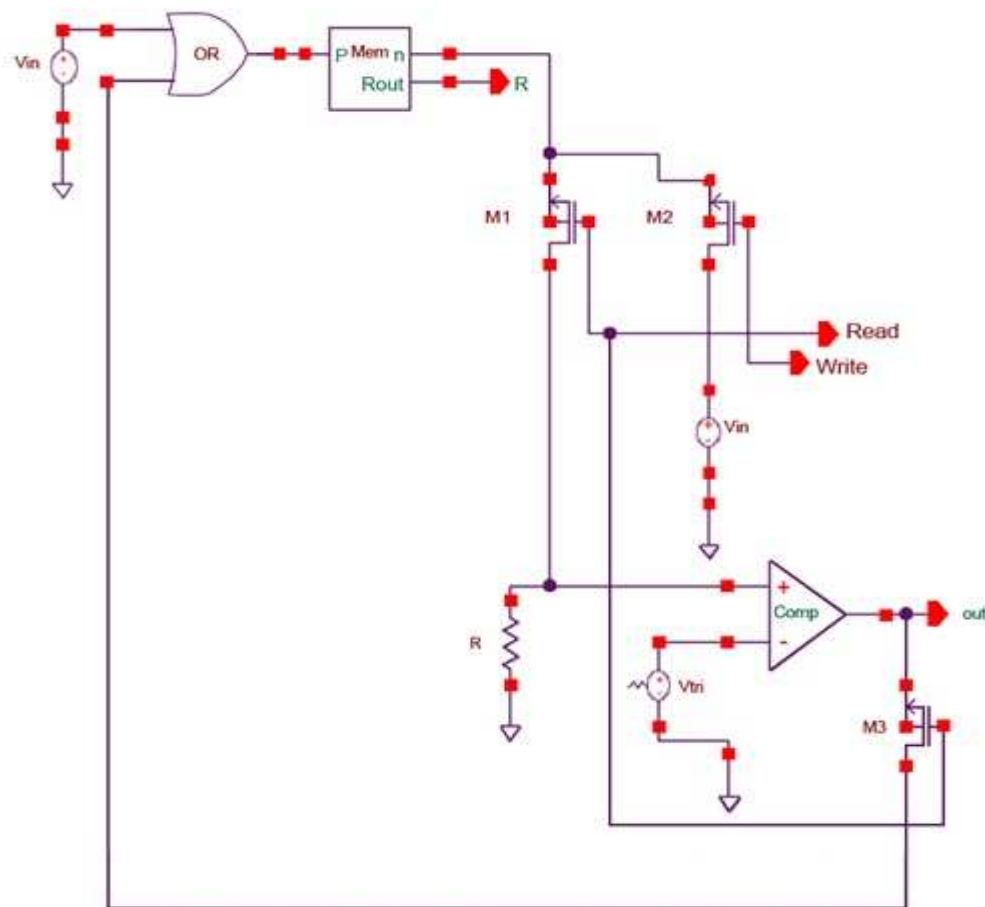
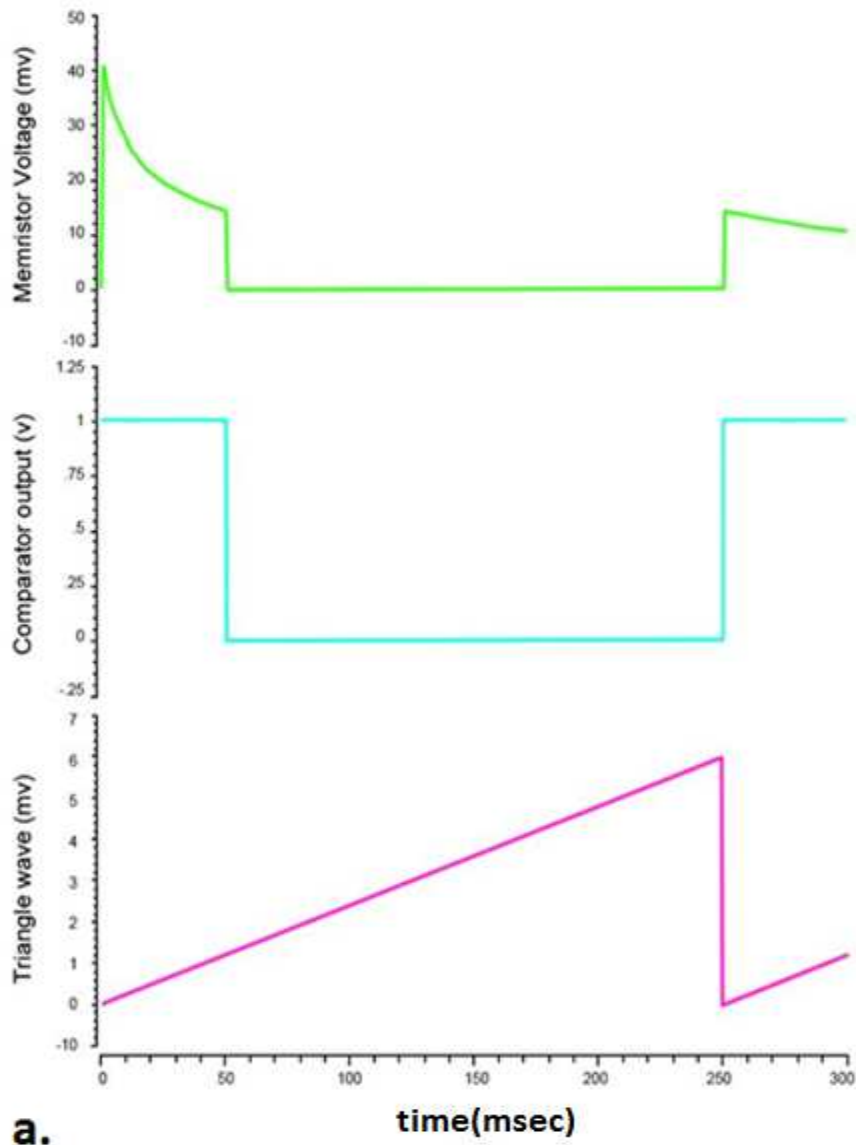
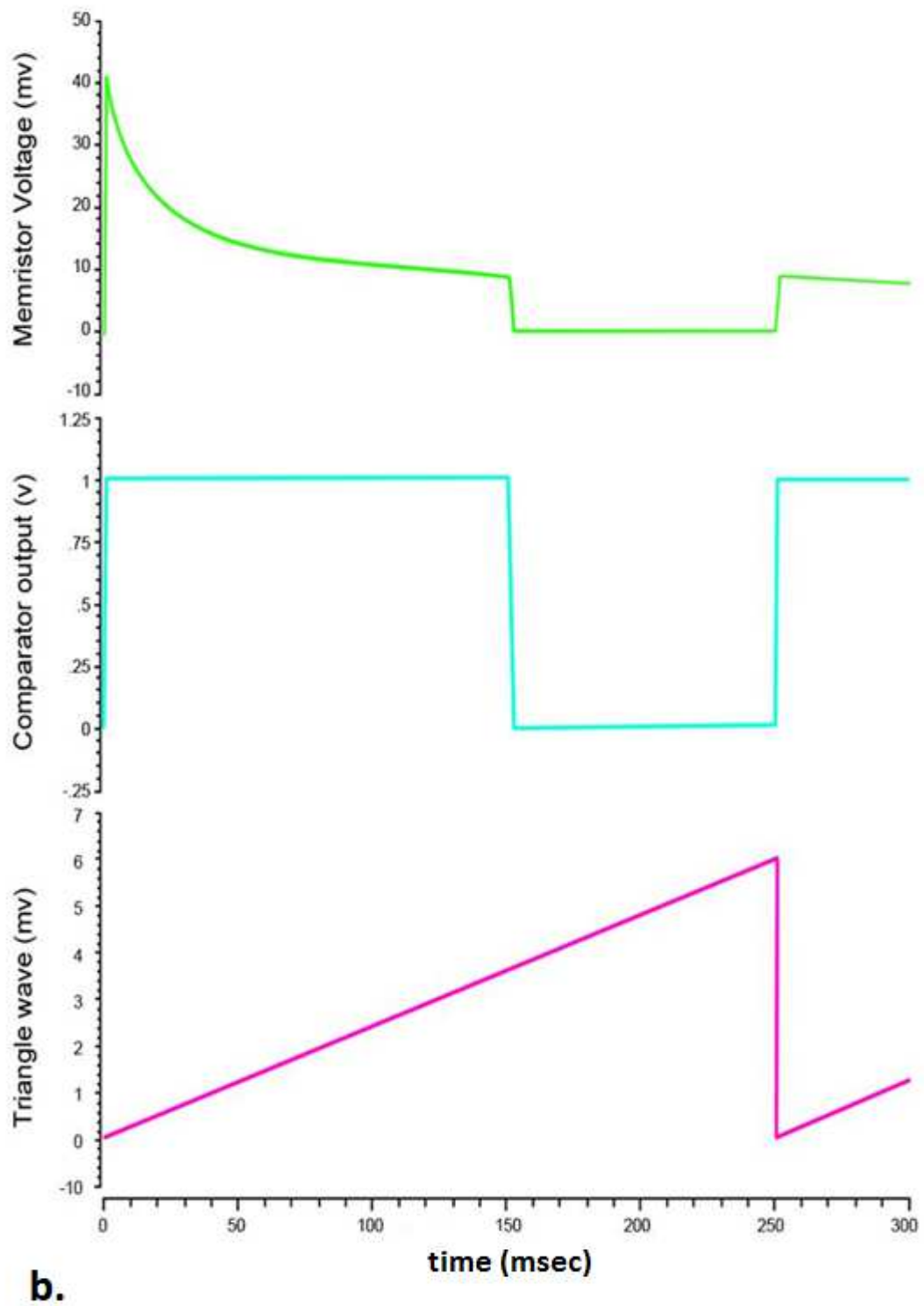


Figure (28) Feedback circuit of read operation

Figure (29) shows the comparator output based on the different resistances of the Memristor. As mentioned before, applying a wider voltage to the Memristor causes less resistivity and leads to a higher pulse at the output of the comparator. Figure (30) shows the complete structure of a non-destructive crossbar Memristor with the feedback circuit.





Figure(29). Comparator output with a) 50m sec input pulse.

b) 150m sec input pulse.

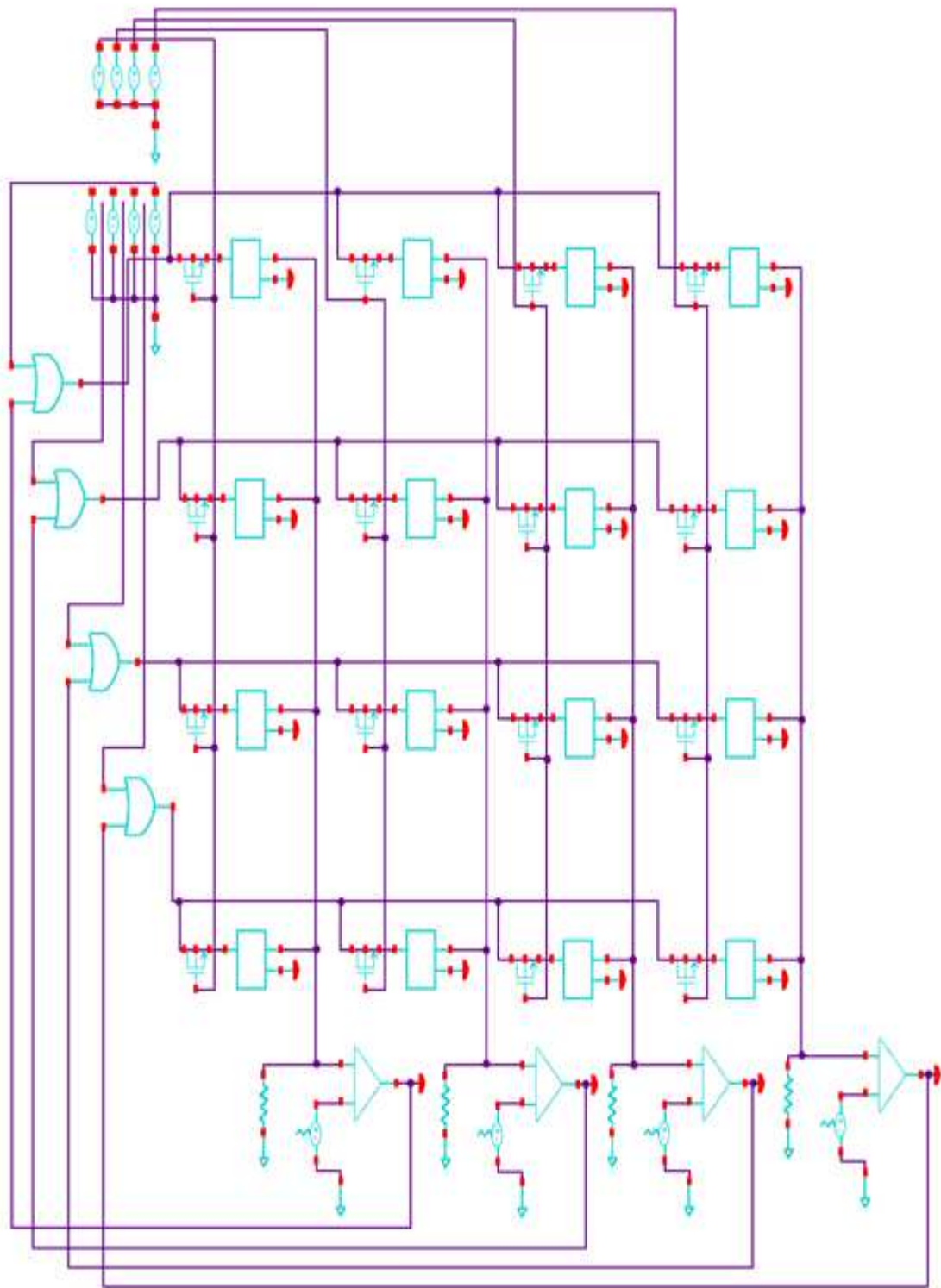


Figure (30) A non-destructive Crossbar Architecture of Multi-Level Memory-Based Resistor (full circuit)

CHAPTER 5

APPLICATION

5.1 Non-volatile memory applications:

Memristors can retain their data even after disconnecting the power supply. Therefore, the first application of the Memristor would be the Non-Volatile Random Access Memory (NVRAM). Memristor can be a good replacement for Solid-State Memories with much faster and cheaper non-volatile random access memory. The HP quantum lab, under supervision of Stanly William, is currently testing a 3nm Memristor [31] which shows the Memristors to be extremely small devices compared to the existing technology. The possibility of stacking several layers of the elements on top of each other enables us to have a higher capacity of the memory with the same area. In addition, by applying different pulses to the Memristor, we can store more than two values in one single cell. This feature of the Memristor will increase the capacity of the next generation of the memories [26].

5.2 Low power applications:

“Flash is becoming more and more fragile so it can’t be written and erased many times. Memristors could be the alternative. And since memristors consume less power than flash memory, inserting memristors into phones, cameras and ultimately PCs could

significantly increase the battery life of these devices”[29]. Based on William’s declaration, Memristors can be good replacements for low power applications.

5.3 Memristor in analog:

In the traditional method, the combination of inductor and capacitor is used to create a Voltage Controlled Oscillator (VCO) which mostly controls the Phase Locked Loop (PLL). PLLs are the main parts of the clock system which are important in each and every digital circuit. VCOs consume a significant amount of energy and occupy a considerable area on the chip. To solve these issues, Memristors can be good alternatives. A combination of the Memristor with inductor and capacitor can create a Memristor VSO which is smaller and has a low power compared to the traditional VCO [27].

5.4. Memristor in Neuromorphic:

One of the interesting features of the Memristor is that it acts just like a human brain cell. In the human brain, neurons are the processors of the brain which are connected by some links named synapses. We can consider the synapses as a two terminal resistance that can be controlled by the neurons (like the Memristors). As mentioned, Memristor can retain its data and recall its previous state just like the human brain cell. This feature leads us to have a computer which does not need to be rebooted every time. “You could leave all your Word files and spreadsheets open, turn off your computer, and go get a cup of coffee or go on vacation for two weeks, When you come

back, you turn on your computer and everything is instantly on the screen exactly the way you left it"[30].

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

Non-volatile Memories play important roles in many electrical devices such as computers and mobiles used as data storage. In addition, there is a huge demand on Non-volatile memories due to their portability feature. As a result, many researchers are trying to improve the capacity of the existing memory elements by scaling the chip. However, with this existing technology, the scaling of the memory became very challenging and almost impossible to go beyond the current technology. Therefore, there are a lot of studies as of recent to find out the alternatives for the current memory element. The missing fourth essential element provided by Chua in 1971, was introduced as a good replacement for the current Non-volatile memory element. This is because they have the advantage of a small size (HP reached 3nm Memristor)[31], they consume low power and they can be used in the crossbar architecture leading to a very dense Memory subsystem. The use of the Memristor is not only limited to the Non-volatile Memories, but also many other applications such as Neuromorphic and logic operations. There are some challenges to fabricate the memory array using the Memristor because of the destructivity feature of this structure. In this work, we proposed a new design to address the destructivity of the Memristor crossbar array. We used a feedback circuit in order to retrieve the Memristors' data after the read operation which led to a non-destructive Memristor crossbar array and a decrease of the read operation failures.

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VITA

Graduate School
Southern Illinois University

Seyedmorteza Sahebkarhorasani

Morteza.sahebkar@siu.edu

Sadjad University of Technology
Bachelor of Science, Electrical Engineering, September 2011

Thesis Title:

A NON-DESTRUCTIVE CROSSBAR ARCHITECTURE OF MULTI-LEVEL
MEMORY-BASED RESISTOR

Major Professor: Themistoklis Haniotakis

Publications:

[1]Seyedmorteza Sahebkarhorasani,"Nano wire Junction less Field Effect Transistor",
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